4 Bit synchronous counter design

Clocking table: Assume the data changes on every rising edge of the clock.

clk	B3	B2	B1	B0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Logic: Bit B0 is simply a toggle FF
Bit B1 changes only if the previous B0 is a “1”
Bit B2 changes only if bit B1 and bit B0 are both “1”
Bit B3 changes only if bit Bit 2, Bit B1, bit B0 are all “1”

Design: (1) Design a toggle flip flop first with a toggle control input. When this Input , tx0 is a “0” FF toggles otherwise not..

First FF is simply a toggle FF
The output of FF1 is connected to FF2 tx0 input.
The output of FF1 and FF2 are NANDed and the NAND output is connected to the tx0 of FF3
The outputs of FF1, FF2 and FF3 are NANDed and connected to the tx0 Input of FF4.

Results: The toggle FF schematic is shown in Figure 1.0. The waveforms of the toggle FF are shown in Figure 2.0

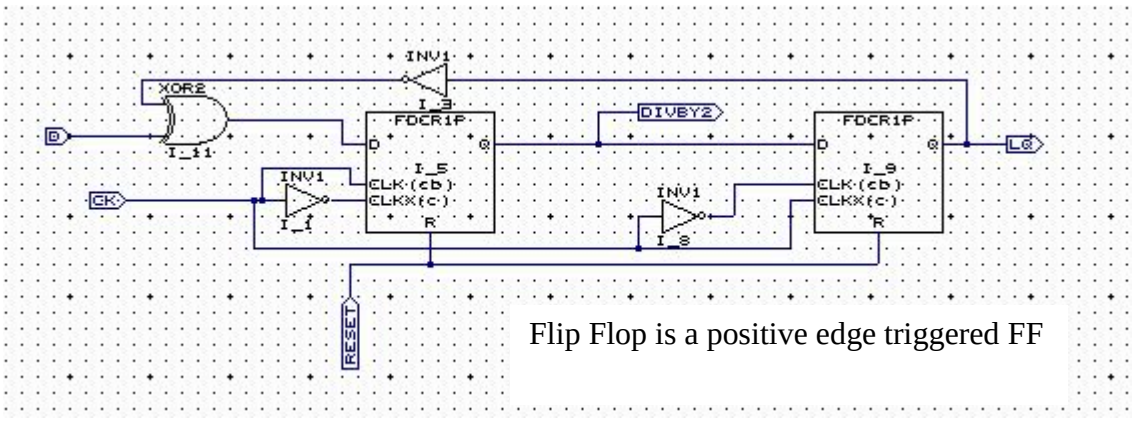

Figure 1.0 The toggle flip flop.

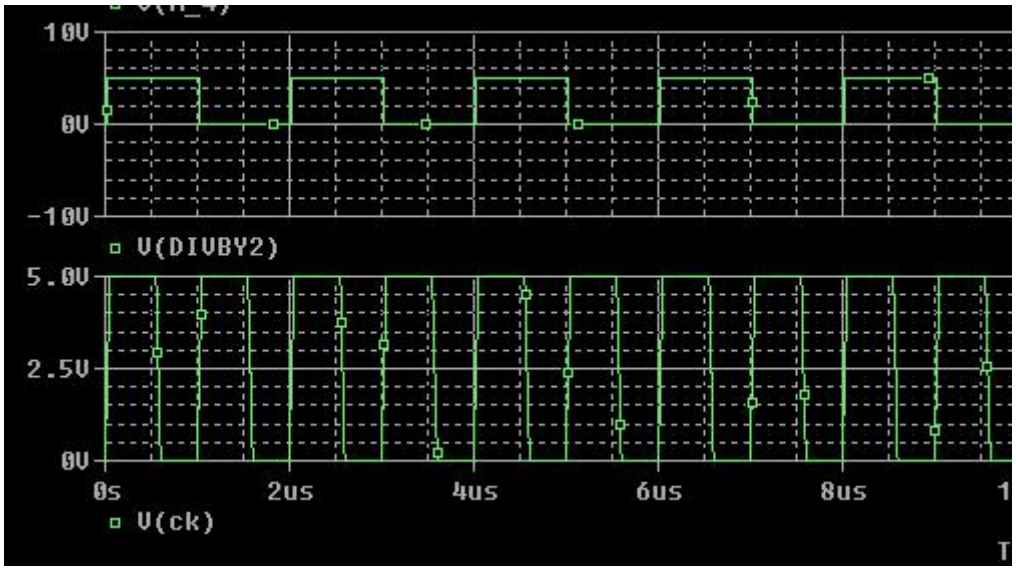

Figure 2.0 Toggle FF waveforms

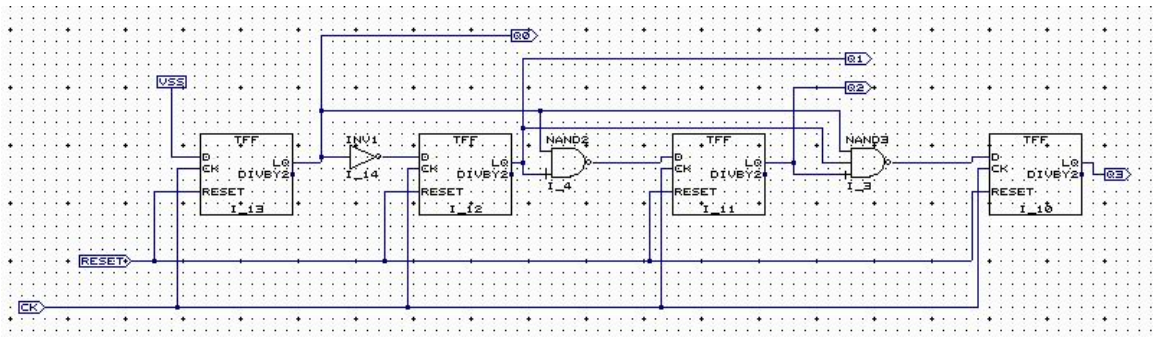

Figure 3.0 The 4 bit counter

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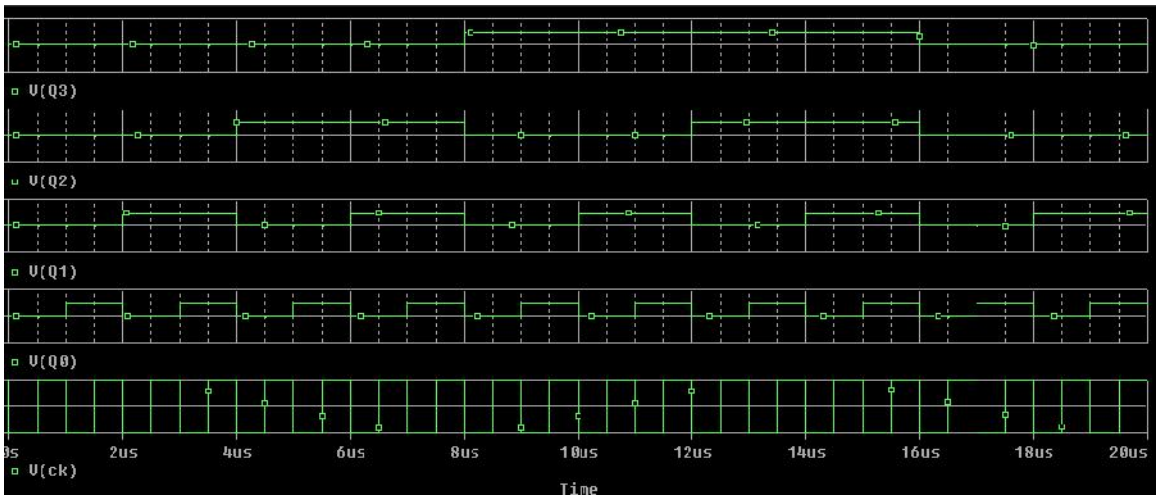

Figure 4.0. Counter waveforms.

Note the trick of using an exclusive OR gate as the gating control.