The All Digital Phase Locked Loop Proposal for Customer. – SPG Technical Staff.

1.0   Introduction: The clock distribution within the customer's Digital Chip relies strongly on de – skewing the regional clock signals using an all digital PLL. We have been tasked with proposing an approach for this ADPLL with respect to the TSMC 0.18um process. A compromise is required so that size, power and jitter may be minimized.

2.0   Specifications: From an analysis of the clock distribution network we have formulated the following specification for the ADPLL frequency synthesizer.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	Operating	1.5	1.8		Volts
Power dissipation	Operating	1.8			mW
Frequency Range	Operating	1		100	Mhz
Frequency Spacing	Operating	67.5			KHz
Reference Frequency	From master clock/divider combo		1.08		Mhz
Master Clock Frequency		200		400	Mhz
Jitter		0.100			Ns
Damping factor			0.707		
Voh	Ioh = 40u	1.2			Volt
Vol	Iol = 40u			0.35	Volt
Output Current	Non Buffered			1.0	MA
Operating Temperature		-40		85	Deg C

3.0   Critical Parameters: The critical parameters influencing the performance of the ADPLL are the configuration of the logic blocks

and filters as well as the response of the semiconductor process to variations in processing, temperature, supply voltage and noise.

4.0   Choice of configuration: We have investigated a number of configurations for the ADPLL. The first case was a simple k –counter ADPLL with a first order filter. Although this was a simple design consuming minimal power and very noise resistant, it was difficult to control the noise parameters to the level we wanted it to be. We then investigated a second order version which used a second ADPLL in the loop. In this case the capture time was significantly large for the amount of allowable jitter. The power consumption also rose quickly when the resolution of the PLL was increased. For these reasons we eliminated this configuration from our choice.

The second configuration we investigated was a variation on the k – counter PLL which included a frequency synthesizer option. This configuration had very good jitter and noise rejection of jitter but the price paid for the performance was power (~ 50mW) and silicon area. We therefore rejected this also.

The third configuration was an ADPLL synthesizer designed specially to de-skew clocks for a very large microprocessor and in use in millions of production devices. This configuration is very common mode noise resistant and has low power as well as self correcting jitter circuits. However it consumes large silicon area. Also the filter section is hard to program easily. It also takes a rather long time to lock. Thus we rejected it.

Ultimately we fell back on the very standard DCO/Digital Filter configuration as originally proposed by the customer with some modifications. This report deals with the analysis that was carried out to arrive at the configuration we are proposing which seems to be a fair compromise and also has a very good chance of meeting the specifications above.

We will also need a reference frequency divider to generate our reference clock of 1.08 Mhz. This is an extra block in the digital chip. The input will be the 50 Mhz reference and the output will be 1.08Mhz.

The analysis results below show the due diligence done on this configuration as well. The conclusions are also presented.

5.0   Process issues:

The process to be used is the 0.18um CMOS process from TSMC. The features of this process most relevant to the digital circuits has been described elsewhere in these studies and is summarized below:

5.1	Minimum feature size:	0.18um (gate)
5.2	Minimum width of active region:	0.22um
5.3	Gate capacitance/area:	50E-4 pF/um^2
5.4	Channel area for min size transistor:	.0396um^2
5.5	Gate capacitance per min size transistor:	2.0E-4 pF
5.6	Maximum Supply Voltage:	1.8 Volt
5.7	No. of interconnect metals:	6
5.8	Interconnect factor	2.5

(Note to get area of the complete active macro-cell, first calculate number of active devices and their area, then multiply by 2.5 to get overall device plus interconnect area for this process.)

Please see the clock distribution technical memorandum for the parasitic capacitance and resistance numbers for the TSMC process. The basic device model parameters for the TSMC process such as trans-conductance and threshold are also described in that document and will not be repeated here. With this data and descriptions of the system and circuits we can estimate power and size of the ADPLL frequency synthesizer.

5.0   Noise:

Noise is an important parameter for the loop in its many disguises. This section of the document deals with this issue.

The sources of noise are mainly going to be:

1.0	Thermal Noise
2.0	Device Noise
3.0	Power Supply Noise
4.0	Charge injection noise
5.0	Substrate noise

6.0   Process variation
7.0   Numerical noise

All these sources of noise will play a role in corrupting the
performance of the ADPLL in one way or the other. However, the
saving grace is that an ADPLL is less susceptible to some forms
Of noise than an analog PLL is. We rely on this fact for this design.

The following are brief definitions of each kind of noise:

Thermal noise: All devices, active and passive exhibit thermal noise
because of the random motion of carriers in the channel and
diffusions. This noise is directly proportional to the absolute
temperature of operation. I.e. thermal noise increases as temperature
goes up.

Device Noise: All MOSFETs and diodes exhibit various forms of
device noise. 1/f noise, shot noise, etc etc. Since our circuit is a form
of a sampled circuit, a lot of low frequency noise will be aliased into
the operating regions of the ADPLL so some care needs to be taken
because of the low supply voltages of operation. In general this is not
so critical in circuits running at higher supply voltages. This type of
device noise can be minimized by using larger gate area MOSFETs.
Obviously there is a clear trade-off between device noise, power and
size of the circuit. This trade-off is an engineering decision.

Power supply noise: Power supplies are noisy in CMOS circuits
unless care is taken to bypass and filter the supplies. This should also
be taken into account for lower supply voltage devices. On chip and
off chip bypass would be required. Do not daisy chain power supplies
for analog and digital sections.

Charge injection noise: The large gate capacitance of the TSMC FET
and the fast edge speeds will almost surely inject considerable noise
from node to node.

Substrate noise: The substrate is common to all circuits. For a small
die size, we would like to space devices close together and have a
dense layout. However, small spacing causes more substrate noise to

be coupled between devices. Guard bands will probably be required around the ADPLLs. (The simplest way to cut down sub. Noise)

Process variations: The variation in the process is a kind of noise and can cause jitter in PLLs (via the inverter variations) as well as in frequency dividers and other logic gates. This variation is a part of the physics of the process. In addition variations of the device performance also occurs because of the various voltage coefficients in the process and nonlinear effects in diffusions etc.

Numerical noise: This refers to the noise due to inexact calculations in the digital machine.

We assume that almost every type of noise except for device and numerical noise can be made negligible by proper design and layout techniques. Other noise components will appear as jitter in the system and will have to be corrected or eliminated by the action.
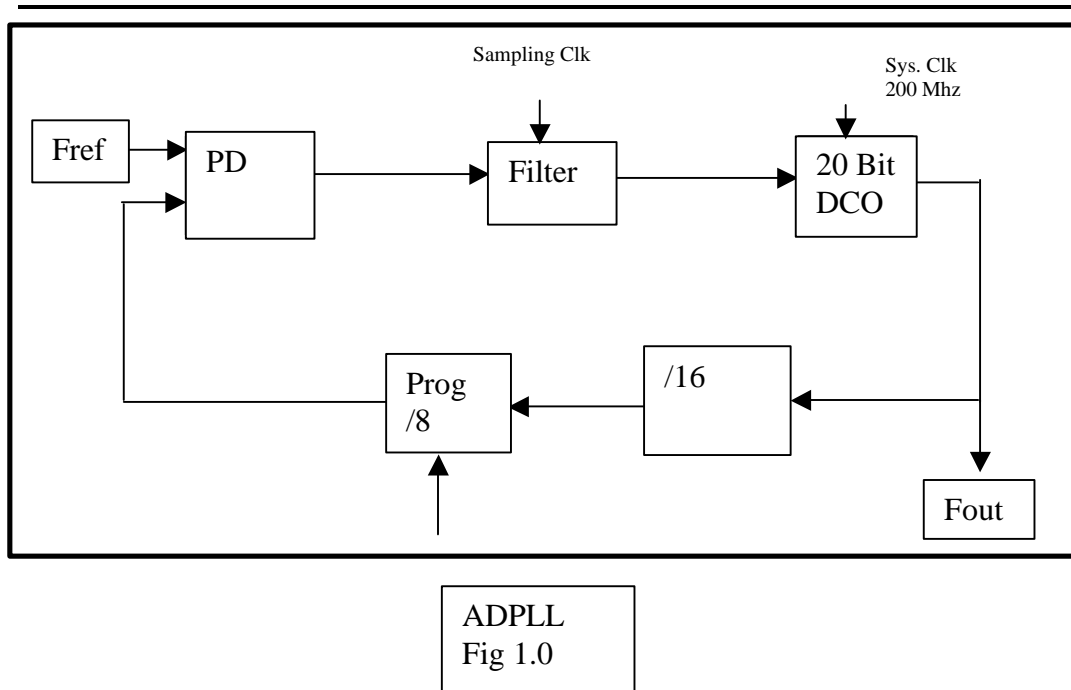
ADPLL
Fig 1.0

6.0   Description of the ADPLL: The ADPLL is based on the standard DCO/Filter combination with a programmable divider for frequency synthesis purposes. The PD is an edge triggered detector which controls the input into the FIR filter. When the reference input

frequency is higher than the feedback frequency the PD generates a logic high and maintains it until the feedback is no longer less than the ref. During the high time of the PD output a continuous stream of 20 bit samples is input to the filter. However, the samples being input are a binary values of 1 when PD is high and a binary value of 0 otherwise. The digital filter is a second order filter whose response is derived from the response of the over control system i.e. the ADPLL. The feedback frequency is based on a reference frequency of 16x 67.5kHz. The programmable divider can therefore generate all the frequencies between N = 14 to N = 192. This allows the system to operate as required.

The design of the system has been carried out by first determining the system parameters. In this case the damping factor and the natural frequency were first chosen to provide stability and settling time of 1.6 usec.
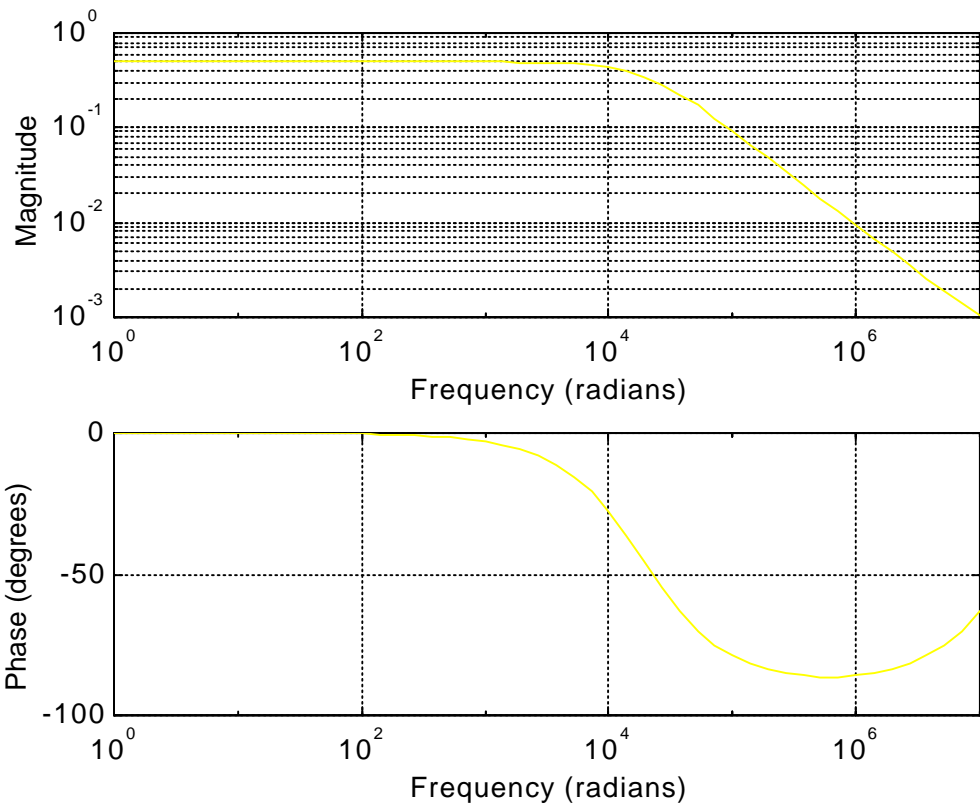
The following system parameters were used:

$$\zeta = 0.707$$
$$\omega_n = 2.65E6 \text{ radians / sec}$$

This provides a maximum percentage overshoot in the transient response of 4.4% which makes the system stable. Using these system parameters generates the frequency response shown below for the overall system.
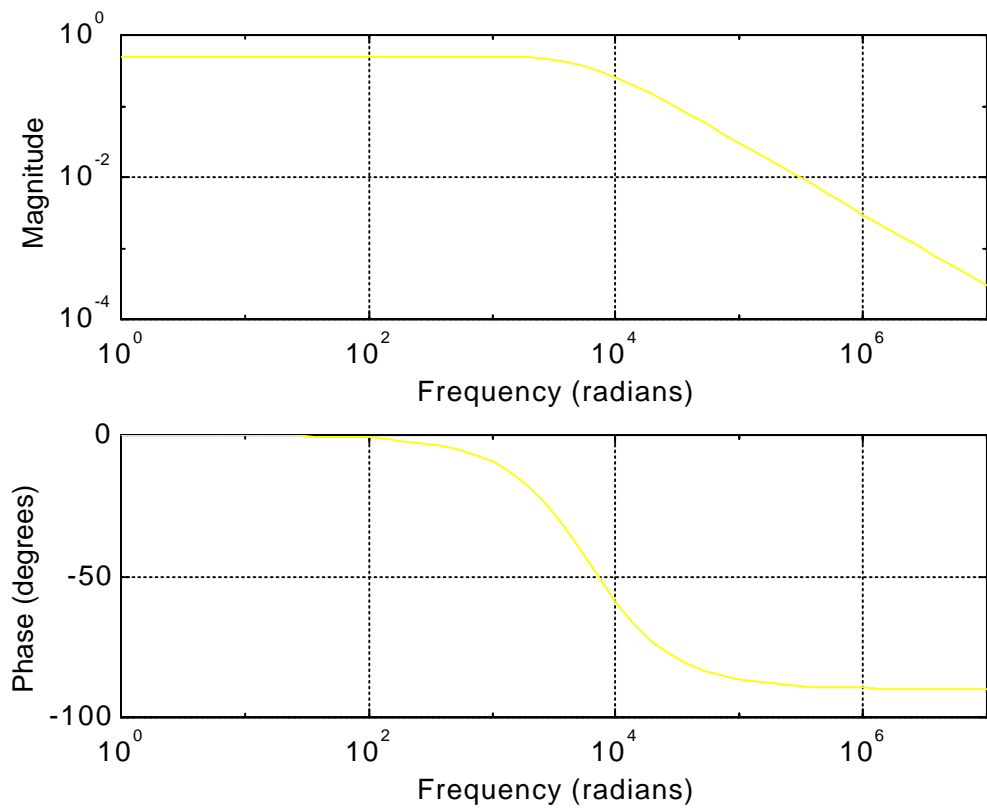
From this overall response the response of the filter is found as shown below:

This provides the filter characteristic. The filter is a second order FIR filter.

The following is the magnitude response of the prototype filter:

-6.0852e+000 1.0000e+000
 -6.0852e+000 1.3895e+000
 -6.0852e+000 1.9307e+000
 -6.0852e+000 2.6827e+000
 -6.0852e+000 3.7276e+000
 -6.0852e+000 5.1795e+000
 -6.0852e+000 7.1969e+000
 -6.0852e+000 1.0000e+001
 -6.0852e+000 1.3895e+001
 -6.0852e+000 1.9307e+001
 -6.0852e+000 2.6827e+001
 -6.0852e+000 3.7276e+001
 -6.0852e+000 5.1795e+001
 -6.0852e+000 7.1969e+001

-6.0853e+000 1.0000e+002
-6.0854e+000 1.3895e+002
-6.0856e+000 1.9307e+002
-6.0861e+000 2.6827e+002
-6.0869e+000 3.7276e+002
-6.0885e+000 5.1795e+002
-6.0915e+000 7.1969e+002
-6.0974e+000 1.0000e+003
-6.1088e+000 1.3895e+003
-6.1307e+000 1.9307e+003
-6.1726e+000 2.6827e+003
-6.2524e+000 3.7276e+003
-6.4024e+000 5.1795e+003
-6.6781e+000 7.1969e+003
-7.1656e+000 1.0000e+004
-7.9753e+000 1.3895e+004
-9.2087e+000 1.9307e+004
-1.0903e+001 2.6827e+004
-1.3009e+001 3.7276e+004
-1.5419e+001 5.1795e+004
-1.8024e+001 7.1969e+004
-2.0745e+001 1.0000e+005
-2.3530e+001 1.3895e+005
-2.6349e+001 1.9307e+005
-2.9186e+001 2.6827e+005
-3.2032e+001 3.7276e+005
-3.4883e+001 5.1795e+005
-3.7734e+001 7.1969e+005
-4.0584e+001 1.0000e+006
-4.3428e+001 1.3895e+006
-4.6263e+001 1.9307e+006
-4.9078e+001 2.6827e+006
-5.1854e+001 3.7276e+006
-5.4559e+001 5.1795e+006
-5.7137e+001 7.1969e+006
-5.9501e+001 1.0000e+007

»

The FIR Filter:

The design of the FIR filter is shown below:
First our pass-band is estimated at 0.19Mhz
Our stop band is at 10Mhz with 60 db of attenuation
Our cutoff frequency is $2\pi(0.20035)$ radians/sec
Our transition region is $\Delta f = \Delta\omega/2\pi$ 0.1996 Hz.

We have chosen to design this filter as a FIR filter based on the
following reasons:

Number of necessary multiplications = 0 (in our case.)
Sensitivity to filter coefficient quantization = low for FIR.
Probability of overflow errors = very low.
Stability = guaranteed
Linear phase = guaranteed
Required hardware memory = small
Hardware filter control = simple
Ease of design = good

Using these quantities we have the impulse response of our filter:

$$hd(n) = \sin(0.20035*\pi(n-16))/(\pi - 16);$$

Therefore the 32 tap weights can be calculated from this impulse response.

The hardware:

The hardware for the filtering is made fairly simple because of the fact that
we are using a binary PD control signal. When we are pumping up the
output frequency we have a logic one (and a number one) at the PD output.
When we are pumping down we have a zero at the output of the PD. So the
actual filter operation is as follows:

As long as the PD output is high, simply delay and add the tap weights (*no
multiplication needed since the input is simply 1.)* When pumping down
make the delays and the additions to be 0. So all we need is a place to store
the tap weights. It could be a lookup table anywhere. Delays are simply unit

clock delays. We will need a 20 bit adder and a scaling circuit to convert the output of the filter (0<o/p<1) to a suitable 20 bit word for the DCO.

The following is an estimate of the hardware size and power needed for the FIR filter.

Hardware blocks:

1.0   Input sampler
2.0   Input register
3.0   20 Bit adder with result storage register and delay
4.0   Counter
5.0   Gating block for output control
6.0   Look up table for taps
7.0   Look up table for DCO control word

Size estimate:

Block 1.0	129 micron squared
Block 2.0	2418 micron squared
Block 3.0	688 micron squared
Block 4.0	250 micron squared
Block 5.0	120 micron squared
Block 6.0	2500 microns squared
Block 7.0	3500 microns squared
Total for filter:	approximately 37.5 mils squared

Operating power estimate (assuming worst case everything works at 50Mhz.)

Total number of transistors using density for 0.18 micron TSMC process:
We get the number of total transistors ~= 4000 (worst case).
The input gate capacitance of each minimum size transistor is = 2.0e-4pf.
Therefore 4000 transistors have a total gate cap of ~ 1pf. (worst case, averaging over size, including buffers. If this is done we estimate about 5pF)
The supply voltage is 1.8 Volt
The frequency worst case is 50Mhz.
Therefore the power is = 5pF*1.8*1.8*50e6 = 810uW/ filter.

Other structures:

A detailed explanation of the other structures has not been provided because they are well know constructs. We will need a edge triggered PD, a 20 bit DCO, an 8 bit divider (programmable) and a 4 bit fixed divider, as shown in the block diagram.

The master clock frequency is assumed to be 200 Mhz.