Clock Distribution Memorandum for the Customer Digital Section Clock Distribution Network. – SPG Technical Staff.

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1.0 Introduction: Clock distribution networks for digital VLSI are important if performance is to be optimized and the best of the circuit is to be realized. This memorandum deals with the analysis and recommendations for the clock distribution of the customer Digital Chip.

2.0 Relevant Documents:

2.1 Customer Clock distribution drawing.
2.2 TSMC design rules for the 0.18um CMOS process
2.3 TSMC Process Electrical Parameters for the 0.18um CMOS Process.

3.0 Process Parameter related basics for clock distribution:

3.1 Assumptions: The longest line for clock distribution will not exceed 2 cm
3.2 10% to 15% of random logic (in addition to memory elements) will accept clock signals.
3.3 The resistance and tempco's of the various metals in the TSMC process are:

Metal Layer	Sheet Resistance (ohms/sq)	TC1	TC2	Resistance Tolerance
M1	0.078	3.43e-3	-1.08e-6	0.023
M2	0.078	3.43e-3	-1.08e-6	0.023
M3	0.078	3.43e-3	-1.08e-6	0.023
M4	0.078	3.43e-3	-1.08e-6	0.023
M5	0.078	3.43e-3	-1.08e-6	0.023
M6	0.036	3.60e-3	-1.16e-7	0.009

Note the equal sheet resistance for all metals except M6, which is lower. Its tempco is lower as well.

Therefore using these numbers a 2 cm clock line which is 1um wide (can take 1 mA of switched current) will be :

1570 ohms.

For M6, the same number is:

720 ohms.

The capacitance of a **0.23um M1 line is 0.3786 fF/um** on the field oxide only. The spacing from another M1 line here is 0.23um also.
The capacitance of a **0.28um M2 line is 0.3298 fF/um** on field oxide only. The spacing from another M2 line is 0.28um.
The capacitance of a **0.28um M3 line is 0.3610 fF/um** on field oxide only. The spacing from another M3 line is 0.28um.
The capacitance of a **0.28um M4 line is 0.3225 fF/um** on field oxide only. The spacing from another M4 line is 0.28um.
The capacitance of a **0.28um M5 line is 0.3209 fF/um** on field oxide only. The spacing from another M5 line is 0.28um.
The capacitance of a **0.44um M6 line is 0.4143 fF/um** on field oxide only. The spacing from another M3 line is 0.46um.

Therefore from these numbers we can calculate time constants and delays for the signals on the various metal lines. (See also attached information on the TSMC process.)

In addition, we need to know the gate capacitance of the digital circuits connected to the metal lines. Thus:

Cox= 85E-4 pF/um^2 for 1.8V devices (typical)
Cox = 87.9E-4 pF/Um^2 for 1.8V (fast device); This worst case for time constant of interconnect.

These numbers must be borne in mind for clock distribution. The expectation is that the clock only runs on metal.

3.0 H – Tree:

We are recommending symmetric H-Tree distribution structures for the clock. In this distribution structure, zero clock skew is ensured by

maintaining identical paths from the clock to the clocked register of each clock path.

In this clock distribution we wish to connect the main clock source (i.e. the analog PLL) to the center of the “H”. Then the clock signal is transmitted to the four corners of the H for further distribution. These four connections provide clocks for lower levels of the clock distribution and so on. There can be multiple levels of trees also.

The final destination points of the H – Tree are used to drive the local registers. Or are amplified and de - skewed by local buffers. Therefore each clock path from the source to the final destination has the same equal delay. The delays that result are dependent on process parameters that affect the impedance of the lines and particularly the buffers (repeaters) if any.

The amount of clock skewing in a symmetric H – Tree is strongly dependent on the physical size, process control, numbers of buffers etc.
In a properly designed H – Tree the conductor widths should be designed to reduce reflections of the fast edges. Specifically design the impedance of the conductor (metal only) leaving each branch point to *be twice the impedance* of the conductor providing the signal to the branch point.

In the TSMC process we have 6 layers of metal and therefore any cross-unders can be handled relatively easily as long as the via resistance and contact resistance is taken care of and compensated for.

The total capacitance of the H – Tree will be much higher than a random distribution network. This has ramifications for the buffers from the sources. The buffers need to be designed to provide the drive necessary for correct transmission of clock signals on the tree.

4.0 Power Supply and low power dissipation:

The dynamic power dissipated in the clock network is simply CV^2f, where f is the frequency. This power dissipation may be significantly reduced if the digital chip is run at a lower supply voltage. Not only the clock but the logic as well. If it is at all possible we recommend that it should be. This will reduce, noise and power across the board. The peripheral circuits can and should operate at the higher power supplies of 3.3V and use the 0.3um channel length.

5.0 Process sensitivity for clock distribution:

A primary disadvantage of a clock distribution network is the delay of each of the elements of a clock path that is sensitive to process and geometrical variances that exist in the implementing technologies, in this case the 0.18 um TSMC CMOS process. As device parameters vary the clock distribution network performance will change. Please consult TSMC info for process variances.

We recommend that circuit design techniques be used that are tolerant of process changes. Some of these techniques are described below.

5.1 The first technique uses the fact that NMOS and PMOS devices tend not to track each other. The response times of these devices move in opposite directions. These delays should be matched in the buffers of the clock distribution network. Since this is a standard technique it will not be commented on further except to mention the two rules of this matching algorithm.

5.1.1 Match the sum of pull up delays of the p – channel MOSFET with the pull up delays of any related clock signal paths.

5.1.2 Match the sum of the pull down delays of the n channel MOSFET with the pull down delays of any related clock signal paths.

Note that this technique should be used routinely to make circuits less sensitive to process variations even if the circuits are more complicated logic circuits.

5.2 For automated layout please lengthen specific clock nets equalize length of every clock line and keep clock skew close to zero. Since long thin lines are more sensitive to process variations. Therefore make sure that the width of critical lines is made larger specially at the root of the clock tree. In other words the clock skew is more sensitive to changes of line widths close to the clock source. Therefore this part of the clock distribution network should be of concern.

5.3 Note as line lengths and widths are equalized, line capacitance will change. This must be accounted for in the design of the buffers for the clocks.

5.4 Please use the following equation for calculating clock path delay of lines with a inverter at the other end: (Buffers)

$T = 1.02R_{int}C_{int} + 2.21(R_{Tr}C_{int} +\_ R_{Tr}C_{Tr} + R_{Tr}C_{Tr} + R_{int}C_{Tr})$

Where $R_{int,}$ C_{int} are the interconnect resistance and capacitance. (TSMC values already provided above). R_{Tr} , C_{Tr} are the output impedance of the inverter and the input capacitance of the inverter (Cox . W.L). R_{Tr} = [KP*W/L*(VDD – VT)].$^{-1}$ VDD is supply voltage, VT is the threshold voltage. The values are provided above.

5.,5 Since clock skew variations are a function of the process variations please analyze and correct for this by using a statistical approach to model the variations and thereby reduce the risk of random clock skews. For random clock skew estimation please use the equation below.

$T_{skew} = \sigma (4\ln R - \ln\ln R - \ln 4\pi + 2C)/\sqrt{(2\ln R)}$. Here σ is the standard deviation of a single path delay. Parameters for calculation of this quantity are provided above in the introductory section. R is number of clock signal paths, C=0.5772

$\text{Variance}(T_{skew}) \approx \pi^2\sigma^2/(6\ln R)$

The first equation is assumed to be a worst case (upper bound) on the expected clock skew for a clock distribution network with R signal paths. Note that that the skew grows with the square root of the logarithm of the size of the system. (The number of clock paths). A note on these equations. These equations become more and more accurate if the system is regular. However, the purpose of using these equations is to gain insight and estimate an UPPER bound on the clock skew expected. That is the way these equations should be used.

Again we stress the importance of simulation of a back annotated *layout. Please extract parasitics completely.*

5.5 Off – chip clock skew: Need to try to make clock skew at the I/O pins nearly or perfectly zero in order to avoid complications when clocks and signal go off chip.

5.6 General Comments:

5.7.1 Need to use simulation to make sure that clock skews for any reason does not exceed 5% of system clock period *ever* owing to process variations. (<1.0ns for our design) We estimate that clock jitter of the order of between 0.1ns to 0.5ns should be sufficient for this clock distribution network (global).Local clock skew and jitter is a function of the timing of edge dependent circuits. Yet for the operating frequencies shown in the Customer clock distribution diagram it appears that for the TSMC 0.18um process with inverter delays of 10's of picoseconds a 100ps jitter should be fairly well tolerated.

5.7.2 Need to make sure (see below) clock coupling does not cause problems because of significantly high fringe capacitances in the TSMC process.

5.7.3 Need to make sure that edges do not get corrupted, again as a result of significantly higher capacitances in a small line width process like TSMC 0.18. (Compare 50e-4 pF/um^2 to 10e-4 pF/um^2 for COX for other larger line processes) The fact is that we cannot just narrow the clock lines since the current carrying capability of the metal lines in the TSMC process is almost the same as that for other lower capacitance processes. Therefore the gate capacitances are also going to play a more important role in corrupting clock edges. In fact we will have to broaden the clock lines as has been mentioned above.

5.7.4 Need to use logic islands for clock distribution purposes.

5.7.5 Need to buffer the system clock source as close as possible to the output of the VCO (Analog). See more on the PLLs below.

6.0 Noise margins:

At lower voltages noise margins will be lower therefore low noise techniques need to be used. These include guard banding, metal line shielding, on chip bypass caps., on package decoupling capacitances should be used as conservatively as possible specially in the vicinity of the I/O buffers. The PLL clock source should be placed on the periphery in such a way that it is symmetric with respect to the clock tree and its pads are low noise design pads, otherwise the pads will pick up noise from the substrate and cause errors. Make sure that dummy bond pads are placed strategically on both sides of sensitive I/O for all three PLL's. To reduce any impact of noisy supplies, we recommend that the PLL's should have isolated supply pins and float above ground to avoid substrate noise pick up. There should be guard bands completely enclosing the PLL. All PLL pins should be placed as close to the PLL as possible to avoid voltage variation with signal transition. Care should be taken to insert ferrite beads in the digital power supplies specially those feeding the buffers to prevent clock noise in other sensitive power lines. Bypass capacitors as close as possible to the power pins should be used. Note inductance of the bond wires of the chip will cause noise. Pairs of pins should be provided close together for sensitive pins such as reference frequencies etc. This will provide a wide noise margin. Place either a ground pin or a power pin next to all signal pins if at all possible. Prevent ground bounce by staggering the large current clock drive buffers in clock time.

7.0 Power distribution:

To provide a stable and clean power supply for the clock distribution as well as the logic, the resistance of the power supply lines should be as low as possible. Also decoupling capacitance should be provided on – chip as much as size constraints will allow (> 100pF if possible). To reduce parasitic

resistance which causes voltage drops we need to use at least double layered power supply lines (perhaps 150 to 200 um wide). Please place decoupling gate capacitors below the lines to decrease power voltage variation. Power to the local blocks should be provided on at least 50um lines. Preferable 80um. Limit the voltage drop everywhere on the chip to less than 50mV. The stability of the substrate voltage levels is extremely important so make sure that there are many substrate contacts. There should be a substrate contact no more that 20um from an active device connected solidly in metal. Place shield contacts under the ground lines to stabilize substrate voltage. This produces very significant noise reduction. The ground line is a good noise shield.