Dc offset voltages in an operational amplifier

Introduction: DC offset in differential amplifiers arises from (a) a systemic offset which is caused by current mismatches and bias problems in the circuit including channel length modulation of CMOS transistors (if the differential amplifier is CMOS) and (2) random variations in the fabrication of the transistors include traps in the gate oxide of CMOS transistors. The offset voltages for CMOS amplifiers are the worst while bipolar and JFET input amplifiers have the lowest offsets.

Solutions: In our view solutions to offset voltage problems are multilevel. The simplest solution (when an offset is not too severe a problem and is mainly a systemic offset) is to fix the currents that bias the input and gain stages of an opamp carefully. The better the biasing the lower the systemic offset. The next level up is to use biasing techniques and common centroid layout of the input transistors. Here each input transistor can be split into two and the bases/gates, sources/emitters and drains/collectors of these transistors are cross connected. This helps to reduce the offset due to oxide or implant variations across the device or wafer.

More stringent offset requirements can be addressed by a set of techniques that are complex to design, simulate, layout and build. The first of these is a trimming technique. Here the input transistors currents or vbe/vgs can be trimmed using a DAC type arrangement. The device is trimmed at test time using either polysilicon fuses or metal fuses. The former are preferable. Another trim techniques quite popular a few years ago, was the so-called “zener zap” technique. This technique involved a series of zener diodes which could be zapped with a power strobe and their post zap voltage would be well known. This voltage could be used to trim the input offset.

Latterly floating gate (non volatile memory cells) have been used to set the offset voltage correction which lasts for many years and is easier to program. For extreme correction, chopper amplifier techniques are used where the main amplifier is auto zeroed using an auxiliary chopper amplifier that senses the offset of input transistors and continuously adjusts the offset voltage trim. Microprocessor based systems also allow offset voltage correction using the intelligence the microprocessor brings to the system. An example is a loop that uses digital offset extraction and storage circuitry, and has an analog current-mode output. Offset cancellation can be performed at power-up or upon request.

Conclusions: Ultimately the type of correction used for the dc offset depends on the type of application and the other parameters of the op amp to be designed. Tradeoffs between complexity (cost) and effectiveness of the offset correction circuitry are of great importance and should be carefully audited as part of the design.
