The Pitfalls of Analog Integrated Circuit Design

Introduction: Analog Integrated Circuit Design has always been regarded as black art. The reason for this judgement is that unlike digital design there are not many mechanized computerized tools available even today to guarantee success of analog IC designs. It is a truism that analog IC design is midway between science and art. The infinite number of levels in analog signals, the performance dependence on slight variations of the process, the severe impact of noise and leakage currents (both items that are extremely difficult to characterize), the influence of external unknown fields, the interaction of external components and boards, the impact of board layout and interconnect, the difficulty of simulation, the susceptibility of analog ICs to slight changes in layout to name just a few items, can cause disaster in an analog IC design project.

Yet, analog designs are attempted and many succeed everyday. Failures though are more common than successes. Even successful designs are an outgrowth of multiple *expert* iterations on the first silicon evaluation and modification. The first silicon on an analog chip should really be viewed as part of the design process, rather than part of the production process. Therefore everyone concerned should always have low expectations of first silicon in analog IC designs. The first silicon is just a way to get more information about the analog chip rather than the result of a - priori data.

This brief paper discusses some of the more common pitfalls of analog design and what to do to avoid them. Every eventuality cannot be covered for obvious reasons but if this paper can even lead to one success it will have met its objective.

1.0 Lack of a clear specification: If the design is done without reference to a clear specification there will always be trouble. The non - existence of a specification will be a cause of confusion in the designers mind and everything else is then in jeopardy. Make sure you have a clear specification. A specification should be in two parts. One is the functional specification that defines external and internal interfaces, signals, impedance and frequencies. The other is the test specification that defines what the user will see at the pins of the device and how the chip will be tested. This specification will be the "goodness" criterion for the chip. Effort spent on these two items will pay for itself many times over in the total time and money it takes to develop the device.

2.0 Lack of well characterized device models: Every foundry and semiconductor fab provides its users with active and passive device models for design. In some cases though, a foundry may not be able to provide models for analog design, just for digital design. A typical example is a foundry not providing models for the n - well or p - well of a MOSFET. Yet for analog design this can be a major source of noise interaction. Models for noise are another case in point. Analog designs are critically dependent on noise models. Without this no one knows what the device noise is and therefore this source of failure is discounted leading to real problems. We can expand on this list but the point, we think, has been made.

3.0 Complete understanding of Foundry Layout Rules and layout: A fab or foundry provides rules for the layout or construction of active and passive devices. In some cases the rules may not be explicit enough to allow the user or the designer to fully understand the ramifications of the rules. For example, in analog design if two matched resistors are to be laid

out they must be placed in the same orientation as close to each other as possible or inter-digitated. Yet in most cases a fab design rule package will not emphasize this point.

Field implants have impacts on the active and passive devices in subtle ways. Yet this point is not underscored in most rules. Interconnect using metal and common point grounding is a must for analog layout yet these will not be part of the rules and so on. Analog layout of low offset operational amplifiers is very different from simple layout of digital or non - critical devices.

Shielding of low - level signals is critical. Yet this is not very well understood. If the analog device is a high frequency or high voltage device the situation becomes even more difficult. All wires are then antennas (this fact is also true in low frequency design but for a different reason. If there are long metallic lines connected to high impedance MOSFET gates, they gather charge during processing. If this charge is not bled off then catastrophic failure can occur during processing leading to low yield or no yield at all) and small fringing capacitance can become significant.

There are untold number of layout related issues like this to contend with. Therefore in analog design much more attention must be paid to layout than for simple digital design. Very careful planning of placement and routing must be done which is also time consuming but if done carefully will pay off handsomely in the long run.

There will be significant substrate noise generated in devices which could have switching circuits imbedded in them (mixed - signal devices). Since in most cases the substrate is the common medium this noise can be disastrous to device operation. Power supply pads should be separated between the analog and the digital sections otherwise there may be interaction between the two supplies. (As an aside we note that ferrite beads can be helpful in isolating digital and analog supplies off chip).

These are a few of the points to consider. However, each analog device is unique, therefore each device layout and layout rules need to be considered separately and the designer must build on the rules already provided by adding specific new design rules applicable to the layout in question. In some cases, for example, minimum spacing may not be enough, or minimum gate lengths may not be enough, etc. etc.

4.0 Circuit Simulation: Circuit simulation for analog devices is a complex and extremely time - consuming affair. Note that 100% simulation can never be done. To do this will require infinite time or infinite computing power. Therefore, the best an engineer can do is to use judgement to define when an acceptable level of simulation has been done. This task is a very, very difficult one. (Not to mention stressful). When does analog simulation become done? The answer is - never! Therefore, the only means to assure oneself that the device will operate correctly is check on real silicon. This means that the only option is a test chip. (Strongly recommended). If this is not an acceptable alternative then the only option is to wait until first silicon, evaluate and then trim. This is the process most often used by analog designers. Therefore our earlier remark, that first silicon is really part of the design process.

The other common mistake is to use tolerance setting on circuit simulators which is too low. If you are using PSPICE or other variant of SPICE, RELTOL has to be set at 1e-6 at the very least, and if there are capacitors or low currents then CHGTOL and ABSTOL must be set accordingly. The problem here is that as tolerance becomes smaller simulation time increases exponentially. Therefore in most cases many engineers will not do this and end up with unknown simulation results. (Capacitors are very difficult to simulate and any results may be inaccurate).

Large and small time constants on the same circuit are almost impossible to simulate on most circuit simulators. The simulator just doesn't know what timestep to set. If it sets a large timestep, fast signals will not converge and a timestep error will be generated. If the time step is set too small large time constants will cause problems. Thus, this is again an area where judgement comes into play. A most difficult problem.

These are just examples of simulation problems that can really cause analog designs to take time or be in error.

Circuit simulation should ideally be done using Monte Carlo simulations. However, if Monte Carlo is done on large circuits it will be almost impossible to complete simulation runs. The reason is Monte Carlo produces so much output that it will overwhelm most machines for relatively small circuits. The only option then is to do multiple simulations using all the corners of the process for all active and passive devices, all voltages, all currents, all temperatures etc. A single circuit may have to run 10,000 times! The time is very long to do this, yet no shortcuts can be taken, since if shortcuts are taken, either the yield will be very low or the circuit may not work at all.

Generally it has been our observation that shortcuts are taken under pressure of timelines and budget. This simply means that both time and money will be wasted. It is far better to take the time to do this rather than add another source of device failure to the overall project.

In other words: It takes a long time to simulate analog circuits, *but it must be done*!! The moral is that if you have to do an analog design under extreme time pressure and take shortcuts you are in for stormy weather. Yet many people will do just that. They will underbid and underestimate times. The result is failure and loss of money and more importantly *time which can never be recovered.*

There are of course other issues in circuit simulation which are dependent on the type of circuit being designed. For example, switched capacitor circuits require a completely new strategy. Sigma- Delta A/Ds and D/As which are so popular today cannot even be simulated on SPICE or ordinary simulators and need a mixture of circuit, SCF and mathematical tools like MATLAB to simulate. This of course is territory for learned papers and will not addressed further.

The final issue is the issue of full chip simulation. It would be very good if the full analog chip could be simulated. However, except for very small chips this just is not possible. Major chips or major analog designs are just not amenable to full chip simulations. Sometimes this may be because they contain elements such as long or short time constants, switched capacitor circuits or other mutually non - compatible building blocks or that they are simply too big. Yet estimates of operation must be obtained. In most cases this is just not done. However, a strategy must be found to do this. Sometimes it is simply characterizing inter-stage impedance and using these as dummy loads or sometimes a subset of the functional blocks can be simulated. In any case not doing these final checks will ultimately lead to failure.

5.0 Effect of External Components: Generally all analog devices need some external components to operate correctly. At the very least very large capacitors cannot be included on chip, neither can inductors. The problem is that capacitors are not really pure capacitors and inductors are not really pure inductors. All these components have parasitic elements imbedded in them. If the design of the analog chip is done without carefully considering the effects of these external components, then although the chip may pass muster at the probe test it just will not work in the system. The impact of the external components may be such as to rob the chip of its operating regime. Therefore before an analog chip is completely simulated it must be simulated

with the external components. This means that accurate models of the external components are required. This process by itself can be a tedious one. Without this procedure of simulating with the external component models the chip may or may not work. The risk is too great, therefore external components must be modeled and the chip interfaces to the outside world must be simulated and investigated with due respect to the external components it needs to operate properly.

6.0 Effect of the PCB (or Hybrid substrate): One of the major sources of failure of the operation of systems containing analog chips is that failure of the designers or users of the chip to correctly design and layout the PCB or substrate on which the chip will rest. Although it may appear that this is a fairly minor task, for analog systems the PCB (or other substrate) assumes a magnitude of importance that may not be the case for digital chips.

At the very least, the PCB should have power and ground planes, instead of power and ground pins. All inputs and outputs of high gain amplifiers must be separated to such an extent that parasitic interaction does not occur, or else the result will be that the amplifier will simply oscillate rather than amplify (a simple example). No large signal carrying traces should be anywhere near sensitive high gain inputs. Fringing fields will wreak havoc on the operation of the chip. The ground system must be carefully thought out in advance. If there are any ground loops or if there are any common mode currents or any interaction between other parts of the circuit the circuit will simply fail to operate. There must be bypass capacitors on power supply leads. Digital power leads must be isolated from analog power leads with ferrite beads if there is any high performance analog circuitry or digital circuitry involved.

These examples show that the PCB is actually part of the analog chip design. The fact is that analog chips cannot be designed in isolation from the external components, the PCB on which it rests and the interconnect used to interface it to the rest of the system.

Also note that even if an analog chip is designed and modeled after a discrete implementation, and even if the circuitry is exactly like the discrete implementation, the impedance levels on the chip will be much higher, since the parasitic capacitances are much smaller. Noise spikes or other interfering signals which were drowned out in the larger parasitics of the discrete implementation will now cause large noise effects on the chip. So a discrete breadboard can only be used as a guide not as an exact model. Therefore the PCB layout for the analog chip must be done with reference to these issues.

Because of these effects and others, we at SPG do not design analog chips only, but analog microsystems. We must by necessity include and consider the chip, its external components and the substrate on which it rests as an active part of the overall design, development and manufacturing process. To not do so will be foolhardy at best. If this is not done, 9 times out of 10 the whole system will fail to operate successfully and much money and time will be simply lost not considering the reputations of those involved.

7.0 Effect of External Electromagnetic Fields: An analog chip must operate in an environment which, at best, is very inhospitable to its operation. More and more there are a multitude of external EM fields that it must operate in. This effect has to be considered carefully. For example, each and every junction of the chip is a miniature radio receiver. Any AM signals will be immediately demodulated by these junctions. If an amplifier is in close proximity, these signals will simply be amplified to produce almost untraceable sources of chip failure. Very high frequency fields will be received by any antennas which are always present in a chip. The resultant affect on the chip will be the same. If the fields are strong enough they may even latch the chip. This kind of failure is the nightmare most analog designers dread because it is so

intermittent that debugging can not even be done, yet the failure mode cannot be explained. Other sources of EM interference can even be produced unknowingly by the very system the chip is to operate in. If there is a fast signal with a fast edge it will also generate wideband noise with the same result as above. Again the point has been made. We must know the EM environment of the analog chip and analyze carefully and take into account, all of these issues.

8.0 Packaging and Packaging Parasitics: In high performance analog circuits the interface to the rest of the world assumes a disproportionate importance. If the chip is packaged then the bond pad, the bonding wire, the soldering capacitance or the solder bumps all have parasitic inductance, capacitance and resistance. Not only do they have these at each pin, but each pin is coupled to every other pin on the package through mutual inductance and fringing capacitance. When the chip operates these parasitics play an increasingly important role in the operation of the chip. In many cases the chip will fail if these parasitics cause coupling into power supplies, sensitive high impedance, high gain nodes or generate ground noise. Therefore, again, a careful assessment of the packaging or the real world interface must be made, modeled and simulated if a good design is to be developed.

9.0 Conclusions: A number of pitfalls of analog chip design have been presented in this brief paper. Obviously these are the ones which are fundamental issues. As everyone knows, it's the problems you can't see that cause most grief. However, it behooves every analog designer at least to pay attention to the fundamentals. As one gains more experience through involvement in the art more and more challenges surface and they have to be dealt with and one learns through experience.

The best way to execute a successful analog chip design is to understand the operation as well as one can. Specify it thoroughly, use the best judgement one can muster, use every tool to simulate as best as one can, understand the peripheral issues and all the harmful influences exerted on the chip by external and internal operation. If possible use test chips to reduce risk and evaluate parameters that cannot be simulated. **SPG offers a low cost prototyping service for just this reason**. On the main chip itself, put in as many test points as possible so after first silicon these test points can be used to probe internal nodes. If possible use more bond pads than absolutely necessary to bring out other critical nodes so that the first silicon becomes easier to evaluate. Do an absolute thorough evaluation of first silicon and then modify. Use trimming circuits, either fuse link trim-able or ion beam trim-able so that a first silicon can be used almost as a test vehicle. *Never underestimate the time or money it will take to design these type of chips if you want a success*.
