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# The development process for ASICs - investments/timelines

The following tasks are done during the development phase of a custom chip or an ASIC whether it is analog, digital or mixed signal. Depending on the type of development, some of these tasks may be done by the customer as part of an internal development process and rest of the tasks may be subcontracted.

It simply depends on the type of chip or ASIC. For example if the customer has already developed a FPGA for a digital chip, many of the preliminary tasks will already be done and the only thing that a outside design/development or fabrication house has to do is to convert FPGA net-lists into a more compact custom chip. ( Mechanistic effort)

At the other extreme is the organization that simply has a concept and nothing more. In this case the outside design house or development organization has to do all the tasks listed below.

Understandably, timelines and investments reflect these two extremes. There may also be situations in between. Therefore it is very hard to provide generic numbers on timelines and investments. What will be done in this document is to use examples to illustrate the quantities involved.

**Task Summary:**

Exceptions aside, the following are the tasks that must be done when developing the custom or semi-custom IC or micro-system.

1.0 Understanding the Concept.

1.1 Reviewing with the customer and marketing (SPG)

1.2 Writing the preliminary Specifications.

1.3 Reviewing the specifications

1.4 Finalizing the specifications

1.5 System or conceptual modeling

1.6 Modifying the system model

1.7 Reviewing the system model with the customer if any doubts remain

1.8 Finalizing the system model

1.9 Partitioning the entire chip or micro-system or macro-cell to be designed into its functional blocks.

1.10 Understanding each functional block and its I/O loading and characteristics thoroughly

1.11 Designing the functional block or choosing an existing functional block from the SPG library, or modifying an existing functional block.

1.12 Simulating the functional block

1.13 Review all simulations of the functional blocks as the simulations proceed and modify.

1.14 Successively connect functional blocks together to progressively generate the design of the overall microchip and micro-system.

1.15 Successively simulate functional blocks together until the overall system is simulated.

1.16 Document all work done so far.

1.17 Review simulation results in detail.

1.18 Modify design and simulation if needed as a result of the review.

1.19 Finalize schematic and simulation results.

1.20 Finalize all documentation on the design thus far.

1.21 Make multiple copies of all documentation for archiving in multiple places for security.

1.22 Generate or verify that technology files are available for layout and that all information in these technology files is current and correct.

2.231 Generate a floor plan for the microchip or micro-system.

1.23 Layout each functional block from the schematics.

1.24 Run Design Rule Checks (DRC) on each functional block.

1.25 Run Layout to Schematic (LVS) on each functional block.

1.26 Run checks to see that all I/O Nodes and power supply nodes are labeled.

1.27 Run checks to make sure that the layout will be compliant with the particular function the block must perform.

1.28 Successively connect the layout of the functional blocks with respect to the floor plan to generate the overall layout of the chip.

1.29 Continuously run DRC and LVS as the functional block interconnect is being done.

1.30 After layout is complete document all work.

1.31 Make multiple copies of the documentation for security purposes.

1.32 **Note: All work should be backed up as it is being done on a day to day basis, so that if an emergency were to arise the work done is not lost.**

1.33 Review layout internally.

1.34 Make modifications to the layout if needed.

1.35 Re-document the updated layout.

1.36 Review layout with the customer.

1.37 Modify layout if needed after the customer review.

1.38 Completely document the layout and make multiple copies for security purposes.

1.39 Generate a ring binder or similar package with a documentation of all work done so far ( Schematics, simulation results, layout etc etc.). Make multiple copies for security purposes.

1.40 Finish the microchip or micro-system layout by laying out scribe lines, alignment keys or other on-chip structures as necessary.

2.411 Generate the bonding diagram of the device.

1.41 Generate the extra layers needed by the foundry for fabrication.

1.42 Run final DRC and LVS to check for integrity of the design again.

1.43 Generate a full color plot of the design, large enough so that final visual check can be made for any discrepancies.

1.44 Correct or modify layout if any discrepancies are found.

1.45 Repeat steps 2.41 through 2.44 to check that all modifications were done correctly.

1.46 Generate the GDSII database to be sent to the foundry.

1.47 Run a final DRC at the foundry.

1.48 Correct or modify layout if any errors are found at the foundry.

1.49 Repeat steps 2.41 to 2.44 if necessary.

1.50 Send final GDSII database to foundry.

1.51 Ask foundry to send the database back after reading it in their computers.

1.52 Run LVS on the received database to verify that no errors were introduced in transmission.

1.53 If errors were introduced repeat steps 2.41 to 2.43.

1.54 Send updated GDSII to foundry.

1.55 Start the first silicon fabrication.

1.56 Document all the results of the work done so far and generate multiple copies.

1.57 Design the test fixture for evaluating the chip on the bench.

1.58 Generate the test techniques required to test the device on a probe tester.

1.59 Write the code for probe testing.

1.60 Review the tester code.

1.61 Make modifications to the tester code until correct.

1.62 Document all the work done so far and make multiple copies.

1.63 Send all the prototype packaging information to either the foundry, or the prototype packaging vendor.

1.64 Document the prototype packaging information.

1.65 Determine test equipment required for evaluation.

1.66 Buy, rent or otherwise obtain the test equipment if it is not already in house.

1.67 Set up the bench for evaluation of first silicon prototype.

1.68 Receive first silicon prototype from foundry. If these are wafers, immediately send to prototype packaging vendor.

1.69 Evaluate first silicon prototypes on the bench according to the test techniques previously developed at room temperature.

1.70 If the first silicon prototypes pass all tests, evaluate at extended temperature. If there are failures note all failures.

1.71 Generate report of bench evaluation.

1.72 Review all results first internally and then with the customer.

1.73 If the prototypes all work then proceed to the probe testing of all the available first silicon wafers to determine yield.

1.74 Determine yield and any modifications required to improve yield.

1.75 If the first silicon prototypes fail, make modifications to the design as above and go through entire procedure again.

1.76 Repeat steps 2.70 through 2.75 until prototypes are production ready.

1.77 Document all work.

1.78 Send engineering prototype to customer for field testing and qualification.

1.79 Review results of field testing and qualification with the customer. If all devices pass then ready for production. If there are failures ready for modification and repeat steps 2.70 through 2.75 until devices pass qualification.

1.80 Document all work done and make multiple copies for security.

1.81 Review with the customer and transfer the device to manufacturing.

**DISCLAIMER:** The following timelines and investments are examples only and are not meant as exact quotations. Every chip and every development task is unique so exact estimates should always be obtained.

1.0 Example 1.0: The circuit to be implemented is a digital circuit that operates well within the range of technology to be employed. It is a CMOS chip with about 5000 gates of logic ( a gate is defined as the equivalent of a 2 input NAND gate). It may have up to 68 pins and is packaged in a 68 pin chip carrier.

In this case the customer will do all the development tasks including design, simulation using well known industry standard tools. After this there are two outputs. One can be VHDL code which defines the operation of the circuit or a net-list which defines the types of gates used and their interconnect. These are sent to the outside development house for fabrication. A few samples are needed.

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| Typical investment for fabrication: | $15,000.00 to $ 25,000. |
| Typical time for delivery: | 4 to 6 Calendar weeks. |

The fabricators will not do any testing or evaluation. All other tasks will be done by the customer.

2.0 Example 2.0: The circuit to be implemented is a mixed signal chip with about 5000 gates of logic and also has analog content. There may be several operational amplifiers, voltage references, A/D converters or special critical analog functional blocks. However, there is no especially difficult or complex analog circuitry involved.

In this case the entire circuit will have to be developed. The customer may already have a specification but even so the entire development cycle will have to be followed. The chip may be about 100 to 150 mil on a side fabricated in a medium performance standard technology.

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| Typical time for development including fabrication: | 20 to 24 weeks to engineering samples. |
| Typical investment for development: | $100,000.00 |
| Typical chip cost: | $ 2.00 in volumes of 100,000 Units per annum. |

Example 3.0 In this case we have the outer extreme of IC development and manufacture. The required chip is large and may have up to 10,000 gates of logic and very complex analog circuitry which may include high frequency functional blocks such as wireless transmitters or receivers, VCOs, PLLs and also demodulators, modulators, etc. The chip may be about 300 mil to 350 mil on a side implemented in high performance BiCMOS technology. Obviously in this case the development house will have to do all the tasks listed above to guarantee success.

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| Typical time for development: | 50 to 70 weeks to engineering samples. |

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| Typical investment for development: | $500,000.00 |
| Typical chip cost in a 68 pin chip carrier: | $ 25.00 to $ 50.00 in volumes of 100k units per year. |

As can be appreciated, this list of examples is also listed in order of increasing risk.

Between these extremes there lies a continuum of timelines, complexities, investments and risk factors. Lowering risk and managing it can be best done by understanding why most developments fail and what to do about it. Risk reduction and engineering for success begins at time zero.

Failure to follow standard operating procedures is the reason quoted for 98% of failures in IC development. If procedures are followed and the right amount of time and investment is put in, there is no reason why an IC development should fail. It is the intuitive understanding of these factors that differentiates successful endeavors in IC development and manufacture from the unsuccessful ones.

As far as timelines and investments are concerned, note that *someone* will have to put in the time and investment. In simple cases of development the subcontractor probably requires a very small percentage of the overall time and investment, while the customer puts in the majority of the investment. In the case of complex ICs, the customer puts in the same investment in money and time which accrue to the subcontractor for his/her efforts, costs and profits. The right choice is probably based on an assessment of risk and available expertise or the time and money it may take to build in house expertise if it is not available at the time the IC development needs to take place.