LOW COST PROTOTYPING HANDBOOK

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1.0 Introduction:

Development of custom integratd circuits involves the tasks listed below:

1.1 Specifications: A set of functional and test specifications are written and agreed to by the customer and SPG, or a complete set of specifications is sent to SPG for evaluation and quote.

1.2 System Analysis: A system analysis is done, either on the entire circuit or major portions thereof. This involves understanding the requirements and then modeling the functional blocks of the circuit at a high level of abstraction using tools such as MATLAB or PSPICE. Finally after the functional blocks have been modeled they are connected together to form the entire circuit. This step allows both the customer and SPG to finalize circuit techniques, technologies, timelines, costs etc.

1.3 Quotation: After the system analysis a quotation can be generated. This quotation will be relatively accurate. After some discussion the quotation is either agreed to or some changes can be made until all parties are satisfied.

1.4 Circuit Design and simulation: The entire system is broken down into its functional blocks. These functional blocks are designed using the parameters of the recipe, or process provided by a technology vendor or fab.

After the functional blocks have been proven in simulation they are connected together to generate the schematic of the entire microcircuit or microsystem. In this case a microsystem is defined as the custom chip, any external components it needs to operate and the substrate on which it rests. In analog applications this is the rule, rather than the exception.

The complete set of schematics are reviewed by the customer and SPG, with reference to the simulation results. If the schematics and simulation results are found to be acceptable by all parties, the schematic database is finalized.

1.5 Layout and Layout Verification: During this phase of the task, the circuit schematics developed above are converted to a geometrical database, using multiple drawing layers. These drawing layers represent the masks used by the fabricator to manufacture semiconductor wafers. The functional blocks are first laid out and checked for compliance with the rules provided by the fabrication facility. In addition each functional block layout is checked to make sure that it matches the circuit from which it was derived.

This process is continued until all functional blocks have been laid out and proven to be correct both for process rules and schematic integrity. The process rule checks are called Design Rule Checks or DRC. The checks for schematic integrity are called Layout to Schematic checks or LVS.

After this the functional blocks are connected together to form the entire chip. DRC and LVS is done on the complete chip and if proven correct, the chip database is sent to the semiconductor foundry for fabrication of wafers.

1.6 Test Program: In order to test the semiconductor devices a computer aided test program is required. This is simply software code, written for a particular computer that

drives a wafer level tester. The tests on the wafer are called probe tests. These tests are the first screening of good and bad devices that is done in the production environment. The same test program is also used at a later stage to check packaged devices after packaging.

While the chip is being processed, a test program is developed and verified against the test and functional specifications generated in earlier tasks. The test program is reviewed by all parties. It is finalized upon approval. It will be used during the production stage of the device.

1.7 First Silicon: The first silicon that is fabricated by the foundry is sent to the developers and the customers. This is the absolute first time, that the design has been fabricated and it is not ready for production. The first silicon is simply a vehicle to do further evaluation and modifications on the device. Therefore expectations for first silicon should always be low. The device will probably not function to specifications at this time and in some cases all of it may not be functional.

The reason for this is that analog devices cannot ever be simulated to a 100% level. A 100% level of simulation will require an infinite time because of the number of parameters involved. Therefore the circuit is usually simulated to an acceptable level before release to first silicon and final modifications are done at this stage.

1.8 First Silicon evaluation and modifications: The first silicon is evaluated on the bench by both the customer and SPG. Functional problems are noted and corrected. After all evaluation has been done and all performance related parameters have been modified, the evaluation is deemed complete. The work is reviewed by everyone and if the modifications are acceptable then a new database consisting of a reduced set of masks is generated and sent to the foundry for the final silicon to be fabricated.

1.9 Final Silicon: The modified database is reiterated at the foundry and the final device is tested on the probe tester to analyze yields i.e. the number of good devices per wafer. If all goes well the yield will be high and the device will be ready for production transfer. In some cases, even though the device performs correctly, the yield may be low and a further set of iterations may be required to improve the yield and thus reduce the cost of fabricating the device.

1.91 Packaging: The tested wafers are marked with ink to separate the good from bad devices and sent to the packaging house for dicing (cutting) and individual packaging. The packaged devices are again tested to make sure that none of the devices have been damaged by packaging stress. Good devices are ready for delivery.

Until recently, it was not possible to fabricate devices in low volumes at reasonable prices. However, techniques have evolved for the design and fabrication of devices in low volumes which reduce the cost of the device significantly. Similar commenct sare valid for design also.

This handbook addresses these techniques of low cost microcircuit development and manufacture. *These techniques are not a substitute for full custom complete device development. The low cost prototyping technique allows a customer to check out parts of a circuit or make a microcircuit which is relatively small in size (it may be complex in operation) with a small*

number of active and passive components. The idea is to reduce risk on a larger device or to make relatively inexpensive devices in low volume.

2.0 Technologies Available for Low Cost Prototyping: The following types of technologies are available presently for low cost prototyping through SPG:

2.1 CMOS
2.2 BiCMOS
2.3 High Voltage BiCMOS

The following are the relative merits and demerits of these technologies for custom ICs.

CMOS: Low power, low voltage (typically 3.0 to 5.0 Volt) power supplies. It can provide resistors in the range of 100 ohms to 1 megaohm. The larger the resistor, the more space it takes on the silicon. Therefore the user should really use lower values, say values in the range of 1k to 100k. Absolute tolerance for resistors is about +/- 20% and ratio tolerance of two identical resistors lying side by side on the silicon substrate will be of the order of 1%.

CMOS also provides good capacitors. The values are limited to 1pF to 100pF. Again 100pF is an upper limit and many 100pF capacitors should be avoided as they lead to consumption of silicon area. CMOS capacitor absolute tolerance is about +/-15% . However, the ratio tolerance of two CMOS capacitors lying side by side on a silicon substrate is less than 0.1%. Therefore, for matched circuits CMOS capacitors are preferred.

CMOS also has relatively good vertical bipolars, either npn or pnp depending on the type of CMOS. However, these are all common collector bipolars. The collector will always be connected to the power supply.

Lateral bipolars are also available. These can be quite good and are formed by using a PMOS or NMOS transistor in a lateral bipolar mode. HFE's of 100 and above are common and the ft's can be in the 100's of Mhz.

CMOS also provides the switched capacitor resistor for extremely high values of resistance. However, this is not a continuous time resistor and needs a clock signal to operate. The value of a switched capacitor resistor is calculated as 1/fC. Where f is the clock frequency and C is the clocked capacitance. Since ratio tolerance of matched capacitors is less than 0.1% time constants using switched capacitors can be very accurate indeed.

Noise performance of CMOS is comparable to bipolars beyond about 25 kHz. Below that and at low frequencies CMOS devices exhibit high flicker noise and will be unsuitable for low frequency, low noise applications.

CMOS devices cannot provide large currents. An upper limit for a reasonably sized chip will probably be about 100 mA.

BiCMOS: BiCMOS is an enhancement of the basic CMOS process. It adds a high performance vertical npn to the repertoire of standard CMOS. This vertical npn has a typical ft of about 20 Ghz at HFE's of about 80- 200. In addition the vertical npn exhibits superior noise performance and therefore can be used for low noise applications, albeit at the expense of power dissipation.

In some cases however, there may not be a choice. The other parameters are those of CMOS. Therefore, for high frequency, low noise devices the BiCMOS process is the best choice.

High Voltage BiCMOS: High voltage BiCMOS is a further enhancement of the standard BiCMOS process. It allows operation of the CMOS devices to about 50 Volts but with limited current. The npns in the high voltage BiCMOS process are limited to a BVCE of about 30 Volt. It also allows the mixing and matching of low voltage CMOS with inherent higher speed with the high voltage devices. This process is ideal for devices operating at 30 - 50 Volt. Other parameters such as resistor values, capacitor values, etc. are about the same as CMOS.

3.0 Chip Size Determinants: The whole idea about low cost prototyping is to keep the chip size small. Target a chip size which is no more than 100 mils on a side or 10,000 sq mils. This naturally leads to a discussion of dimensions and chip size determinants.

First, chip sizes are measured in either mils (USA) or mm (Europe). A mm is about 40 mils. A mil is 1/1000 inch. Chip mask database units are microns = 1E-6 meters. To get an idea about what is considered a large chip, medium sized chip and a small chip, at SPG we arbitrarily choose to call a chip that is 250 mils on side (> 6mm) a large chip. A medium sized chip is less than 200 mils on a side (<5 mm). A small chip on the other hand should not exceed 100 mils on a side (<2.5 mm).

To extend this discussion on size, note that a chip has three major sections. The first section is the peripheral section of bond pads. This is usually a ring of bond pads spaced around the chip. These bond pads are typically 5 mils square and spaced 5 mils from each other. Therefore the pitch is 10 mils. Therefore a square chip can have 10 bond pads per side maximum. The next section of the chip is the so - called active area of the chip. This is where the actual circuitry resides. This active area must be spaced about 2 mils from the bond pads. Since this is the case the area for the active circuitry becomes 100 - 7 mils per side. Therefore the active area of the chip can occupy 93 mils per side.

We have chosen to use a 100 mil per side chip as our small chip. This appears to us to be the optimum in terms of low cost and functional performance. Other larger sizes are possible but they may be higher cost than optimum. If a customer does need more circuitry than will fit into a 100 mil chip he/she may opt for a larger chip and pay something extra.

The next question is of course what the sizes of the active components are?

For the low supply voltage processes use the following approximations:

1.0	Full CMOS op Amp with low drive:	120 to 200 mil squared
2.0	Full CMOS comparators:	100 - 150 mil squared
3.0	A single 4 input logic gate (for mixed signal applications)	2 to 4 mil squared
4.0	A positive edge triggered Flip flop:	8 to 10 mil squared
5.0	A voltage reference:	400 to 600 mil squared
6.0	An 8 bit slow DAC:	200 to 500 mil squared
7.0	A 10 bit 10 us A/D	1500 to 3000 mil squared
8.0	A fast 8 bit DAC	2000 to 6000 mil squared
9.0	A 10 kohm resistor:	0.5 mil squared
10.0	A 100 kohm resistor:	2 mil squared
11.0	A 1 pF capacitor:	3 mil squared
12.0	A 10pF capacitor:	25 mil squared

13.0	A 100pF capacitor:	258 mil squared
14.0	A CMOS analog switch:	1 mil squared
15.0	A 1X vertical npn	2 - 5 mil squared
16.0	A 1X lateral npn/pnp	0.5 to 1 mil squared
17.0	High Voltage (> 30 V) opamp:	700 mil squared

Note: Op Amp and comparator sizes are for amplifiers and comparators which drive internal capacitive nodes only.

If your design has devices which cannot be estimated from this list call us at 602 - 892 - 1399 or send e - mail to Mohammad Rehman at mafo@worldnet.att.net for estimates of other functional blocks.

Knowing the sizes of these blocks you can form a good estimate of the total area taken up by your prototype design.

The final step is to multiply the area you obtain from adding these functional block sizes by a factor of 1.35 to get the total size of the active area including routing between functional blocks. If you are going to go for the 100 mil on a side chip, this area cannot exceed 8649 mil squared for the optimum small chip.

Of course you are not limited by area in all cases as mentioned above.

To conclude this section on sizing, the low cost prototyping is really a technique to check out small circuits prior to implementing a large chip for risk reduction purposes, to obtain a low volume of small chips or just to check out ideas or obtain some breadboard devices. It should not be used for large complex chips or for high volumes.

4.0 Availability of Functional Blocks: Over the last 11 years engineers at SPG have worked on a variety of analog projects (and some mixed signal). These projects have allowed us to generate many common functional blocks used in analog ICs. These are proven blocks and are available almost off the shelf. However, our experience has been that not all the blocks can be used as is and some modification must be made to fit these blocks for a unique application.

At this time we are offering a service where our customer can work with us to design his or her circuit with as many of these common blocks as possible. If there are some reasonable modifications to be made to a few blocks we will do them at no cost to our customer. The key word is reasonable and it is well known that, that is a word open to many interpretations.

The only suggestion we can make is that our prospective customer should call or e - mail (phone number and e - mail as above) and talk it over. A simple sketch of the circuit or a free consultation is all that is required to pinpoint what can or cannot be done.

5.0 The development flow for low cost prototyping: With respect to the description provided in section 1.0 above the following development flow is used for low cost prototyping at SPG.

5.1 Specification: SPG will not specifically develop a specification. This will be the customer's responsibility. Therefore there is no cost associated with this item. The customer should be able to develop a fairly good spec. by taking advantage of SPG's free consulting service.

5.2 Circuit Design and Simulation: SPG can provide a number of pre - designed functional blocks. For the low cost prototype the customer should talk to us about his design initially. We can then determine the functional blocks available or provide suggestions how the function could be implemented using the standard blocks available. If a required function is not available then we can modify one or more functional blocks to provide a new functional block, which will hopefully meet the requirements.

Once all the functional blocks are in place the customer can sketch out his or her schematic and send it to us. We will do the schematic capture of the circuit and run a simulation. We will provide the results back to the customer who can approve or make modifications. This process can be continued until the chip meets performance. The point must be made that these prototype chips are really expected to be small and therefore easy to simulate. Large chips cannot be handled using low cost prototyping.

Our preferred method of communication during this stage is e- mail. Graphics and other data is provided using Acrobat pdf files. Of course telephone conversations and FAX are always available. Or in the worst case, a face to face meeting could be held.

In short the customer is the chief designer of the prototype while SPG simply acts as a skilled assistant until the required circuit has been implemented using monolithic technology.

5.3 Layout and Layout verification: Once the simulated schematic is available SPG will layout the small circuit and make the masks.

5.4 Fabrication: The prototype will be fabricated in the low cost prototyping foundry and 10 samples will be delivered. Additional samples will be delivered if requested at a nominal charge per sample which will be provided to the customer.

Note, that no test program will be done. All testing will be the customer's responsibility. SPG can take part in testing or debugging at the customer's request only. This activity will be billed as an extra task not included in low cost prototyping charges.

5.5. Revisions: All revisions of the prototype will be considered new projects and charged at the same rates.

6.0 Investments: The investment required for low cost prototyping is dependant on the type of process/technology and the complexity of the chip. However, typically low cost prototyping costs less than $35,000.00 per device compared to $ 150k to $ 200k for a full custom analog chip.

7.0 Timelines: The usual process cycle is about 8 weeks. This should be added any time taken during the design phase by the customer and SPG. The design phase timeline is of course dependant on the type of design and could be as short as 2 weeks or as long as 8 weeks.

8.0 Advantages: The advantages of low cost prototyping are:

8.1 Low up front cash outlay.
8.2 Reduction of risk in design projects
8.3 Get exactly what you want, i.e. it is a full custom chip. Only small in size and complexity.
8.4 No volume restrictions. One or 100 chips.

Tools Provided by SPG free of charge for our customers: We realize that it is beneficial if our customers have the same software tools that we use ourselves during design and development so that they can track, interact, view or otherwise become comfortable with our work.

In order to facilitate this activity we provide the software tools which are relevant to this activity. These tools include:

The schematic capture and netlist tool (Allows you to capture schematics and make various netlists automatically)

The chip database viewer (Allows you to look at the chip layout)