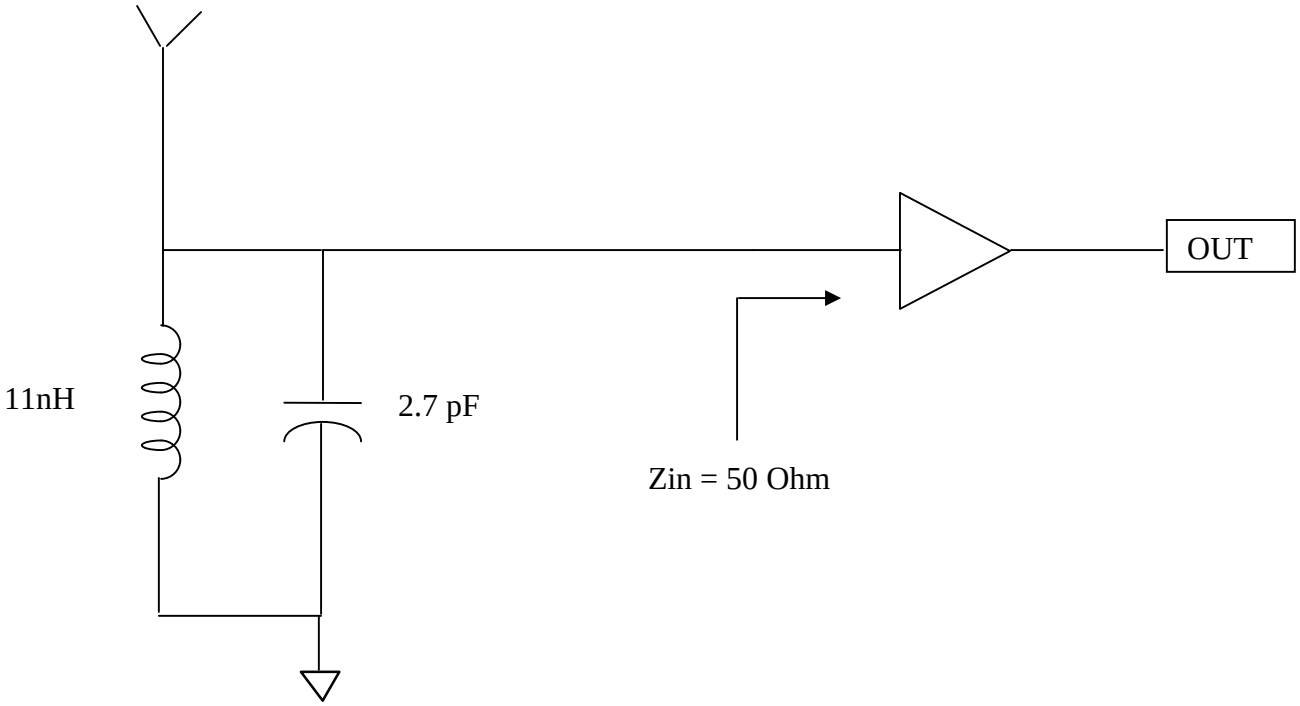
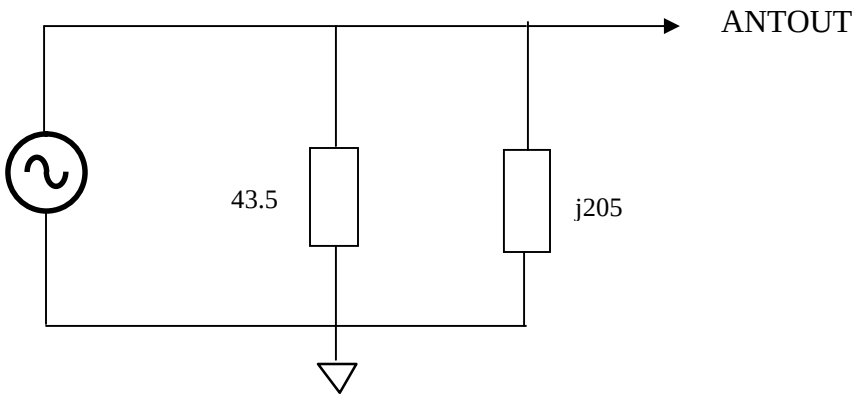
An example in impedance matching

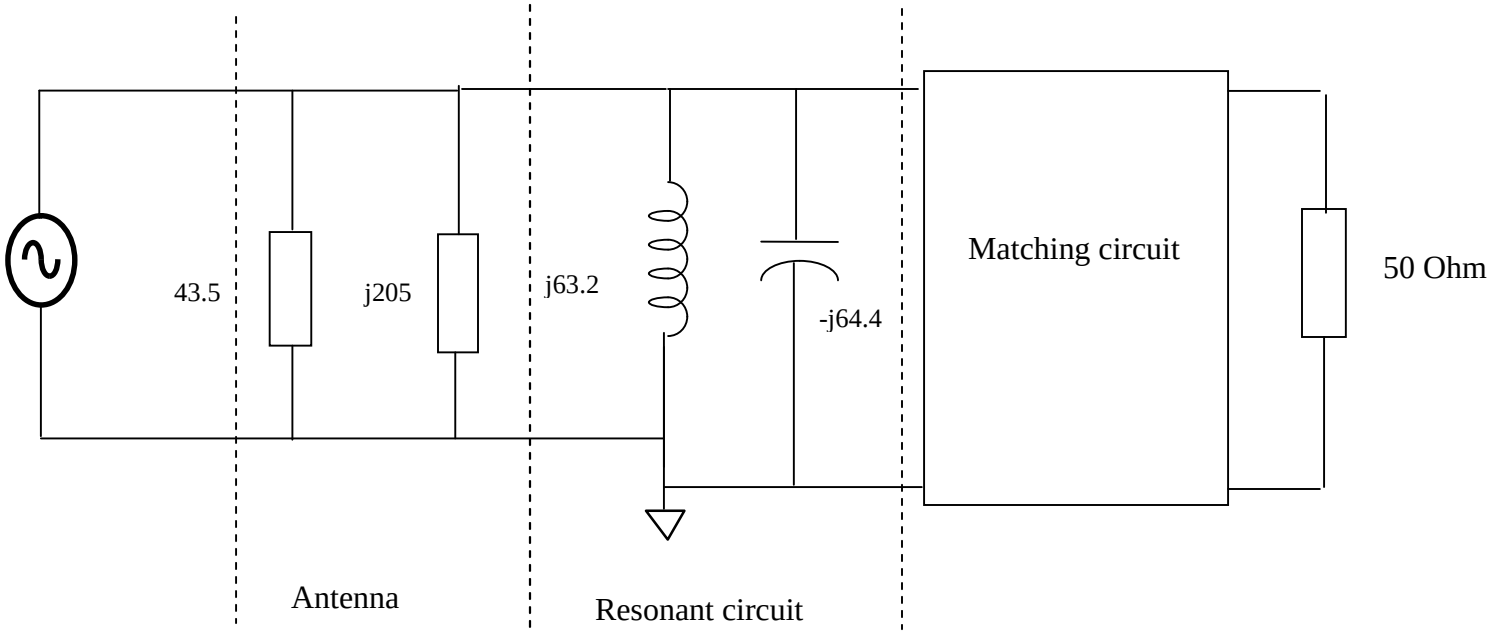
The problem is stated graphically below.



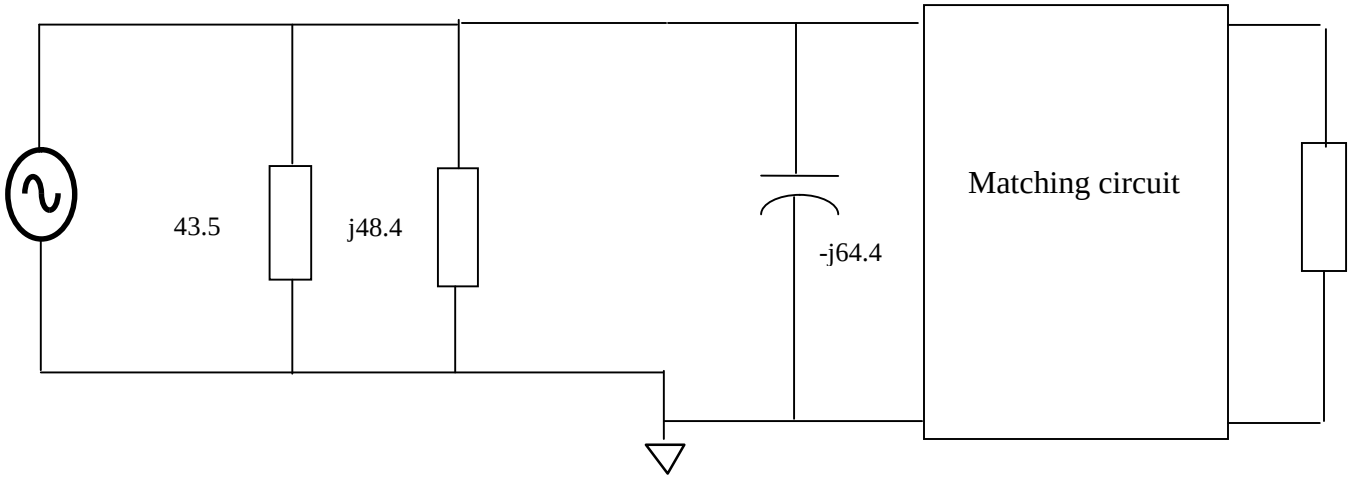
Antenna equivalent circuit at 915 Mhz.



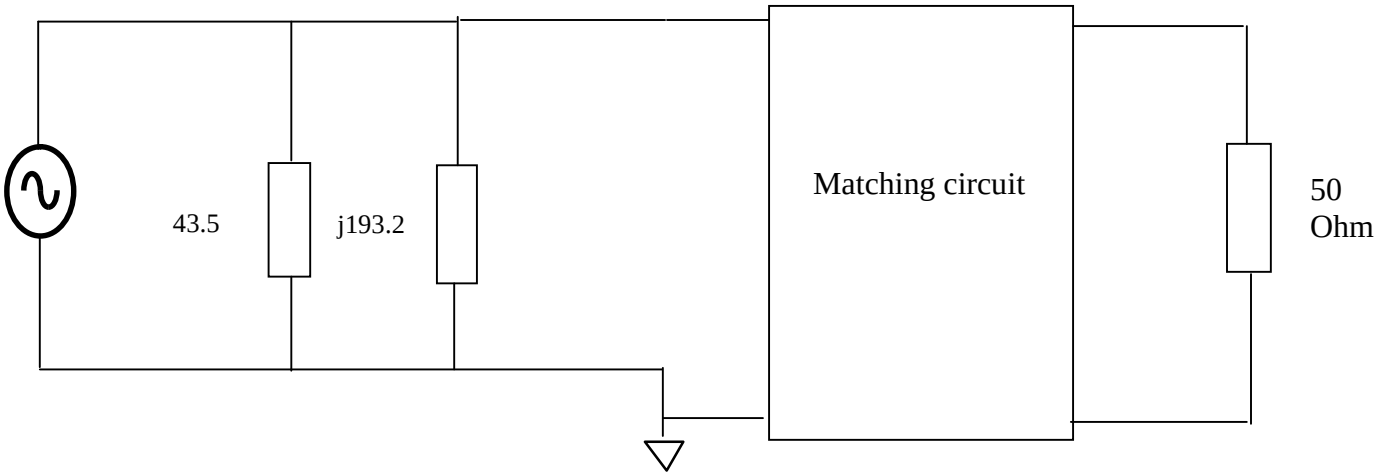
The complete matching problem



The first simplification (combine j205 and j63.2)



The next step – combine j48.4 and –j64.4



Now convert the input parallel circuit to series form

The nodal Q is given by,

$$Q = \frac{193.2}{43.5} = 4.4$$

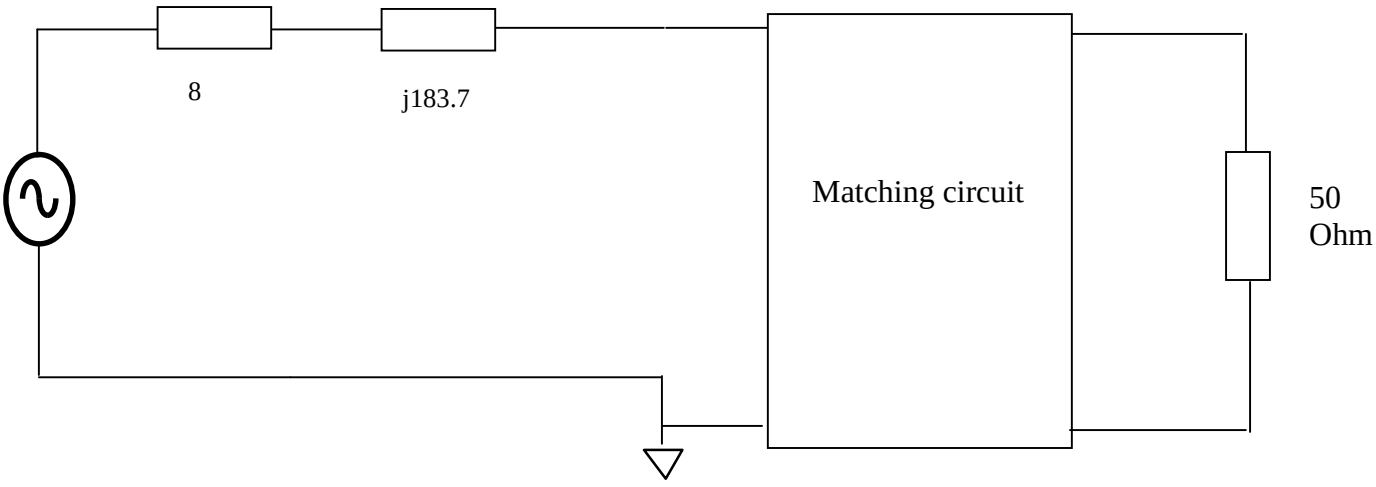
Then R series is given by,

$$\text{Rseries} = \frac{Rpar}{1+Q^2} = 8.0 \text{ Ohm}$$

Also Xseries is given by,

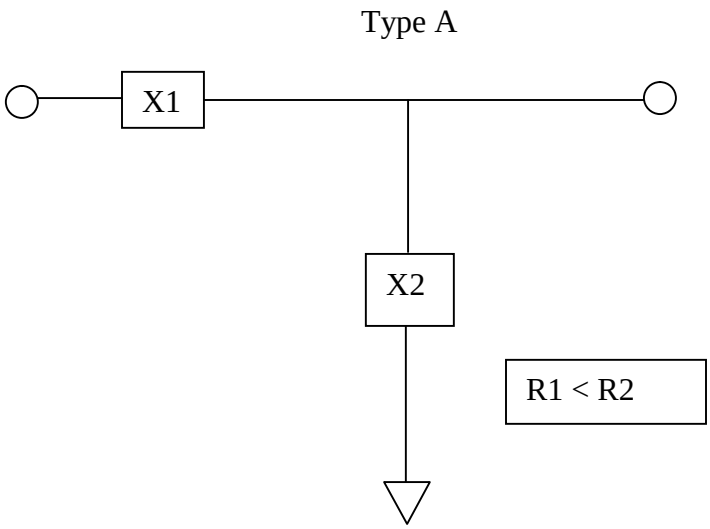
$$\text{Xseries} = Xpar\frac{Q^2}{1+Q^2} = 183.7 \text{ Ohm}$$

This conversion is shown graphically below.



Match 8 Ohms to 50 Ohms using a Type A network

In this case, X1 is assumed to be a capacitor and X2 is an inductor.



The formulas for the matching network are,

Type A network:

$$X1 = \frac{\sqrt{R1R2} - R1\cos}{\sin}$$

$$X2 = \frac{\sqrt{R1R2}}{\sin}$$

Also the phase angle is defined by:

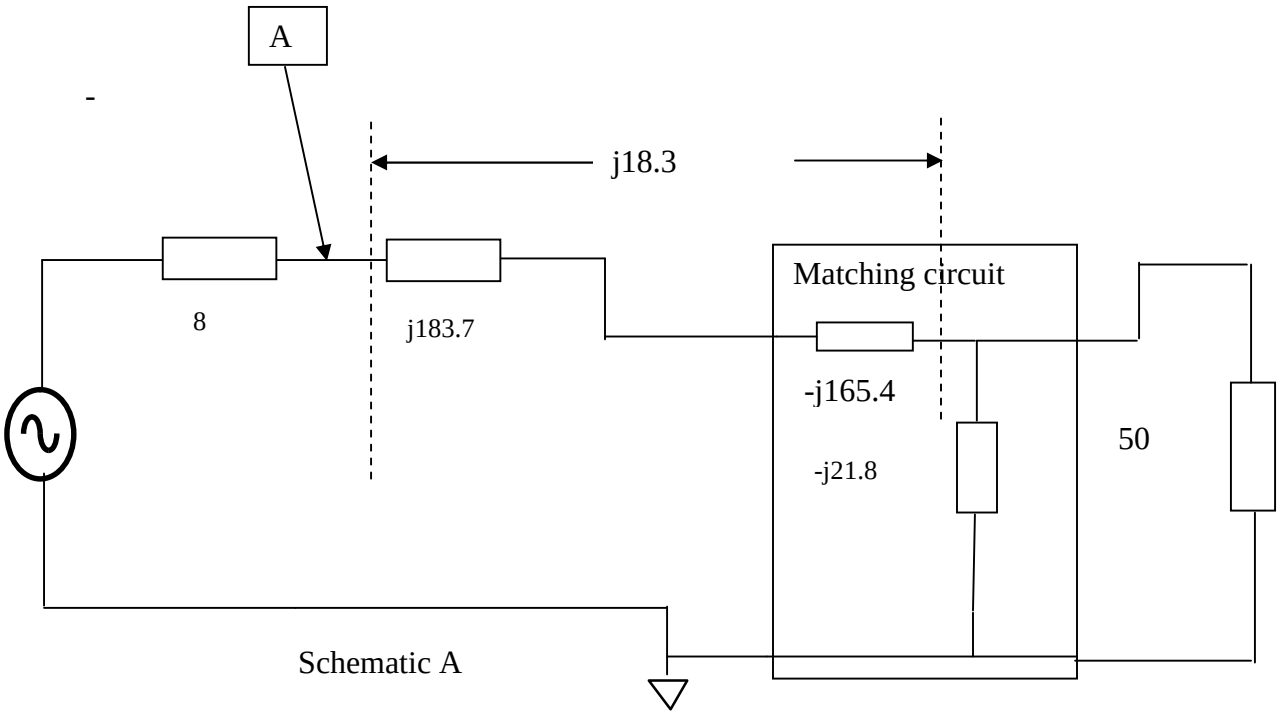
$$\beta = \pm\cos^{-1}\sqrt{\frac{R1}{R2}} = \tan^{-1}\sqrt{\frac{R2}{R1} - 1.0}$$

The phase angle is calculated to be = ±66 degrees
Cos (66) = 0.4
Sin(66) = 0.91

Then,

X2 = -j21.8 and
X1 = j18.3

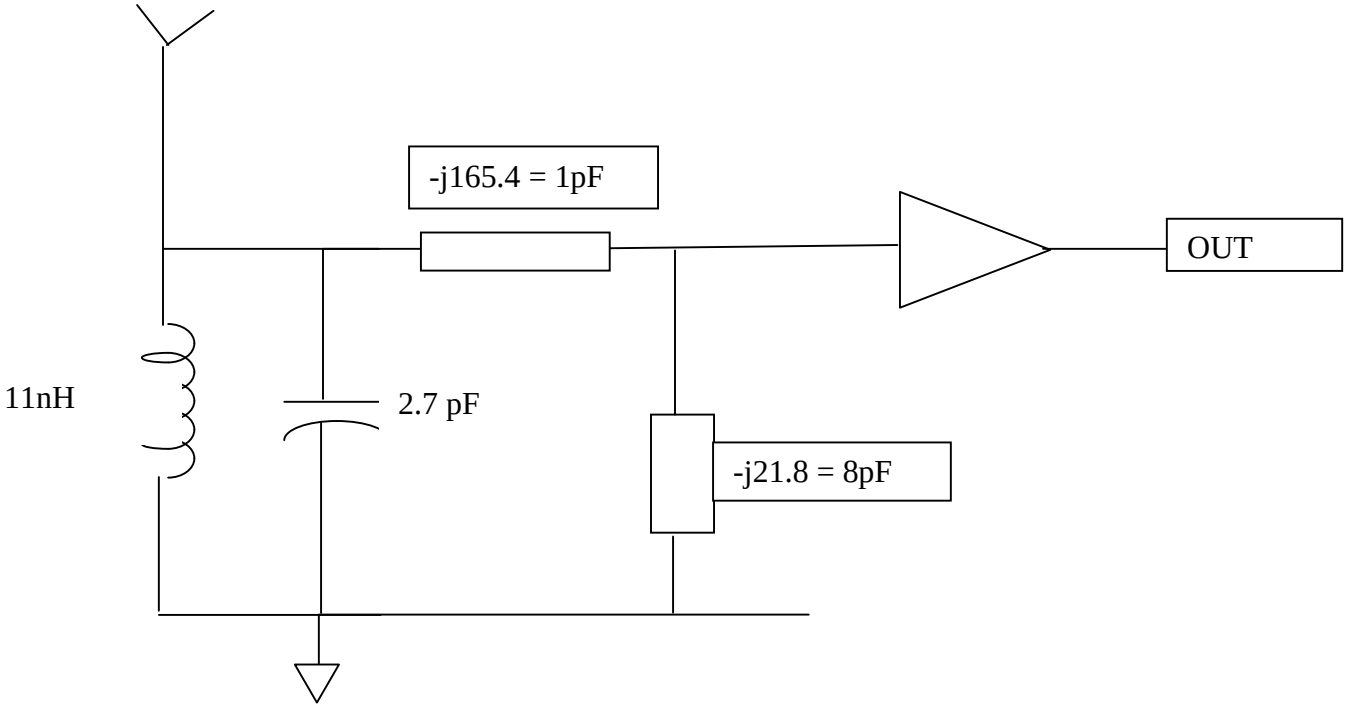
Calculate the matching reactance



Schematic A

From this, the unknown reactance = -j165.4 Thus the matching circuit is a TYPE A, low pass circuit with the calculated parameters.

So we can now show the complete circuit as ,



Now to simulate and test the design. As a check, we convert the 50 Ohm load and the 21.8 Ohm reactance to series. This is done by first calculating the Q. Which is,

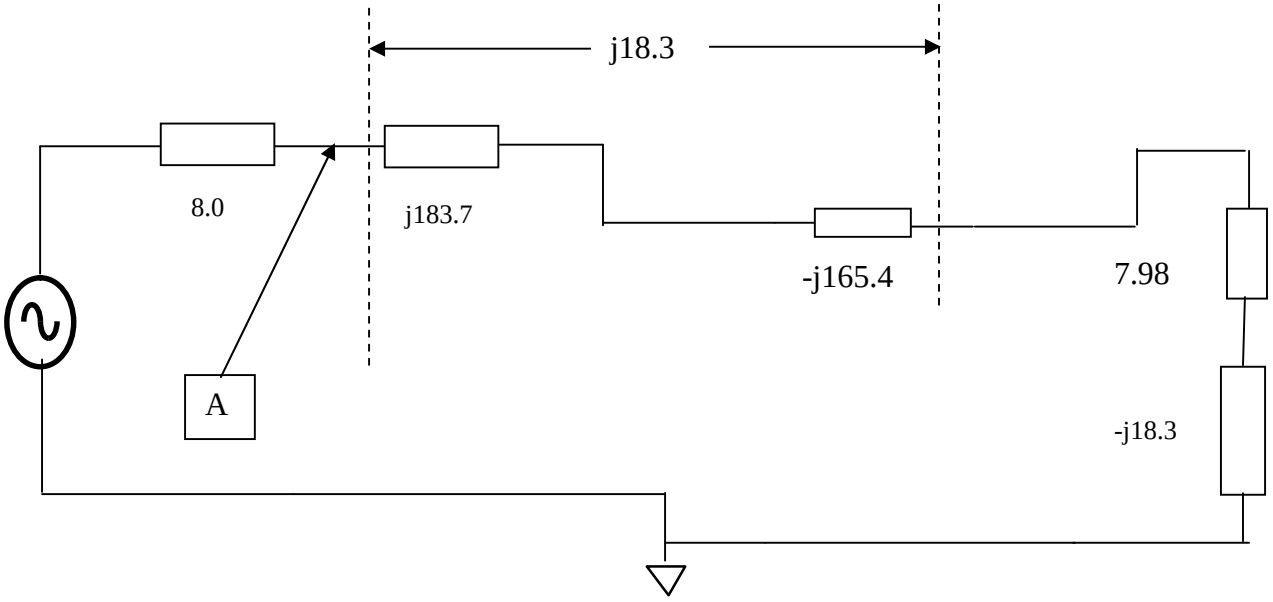
$$\frac{50}{21.8} = 2.29$$

Then the series equivalent of 50 Ohm is,

Rseries = 7.98

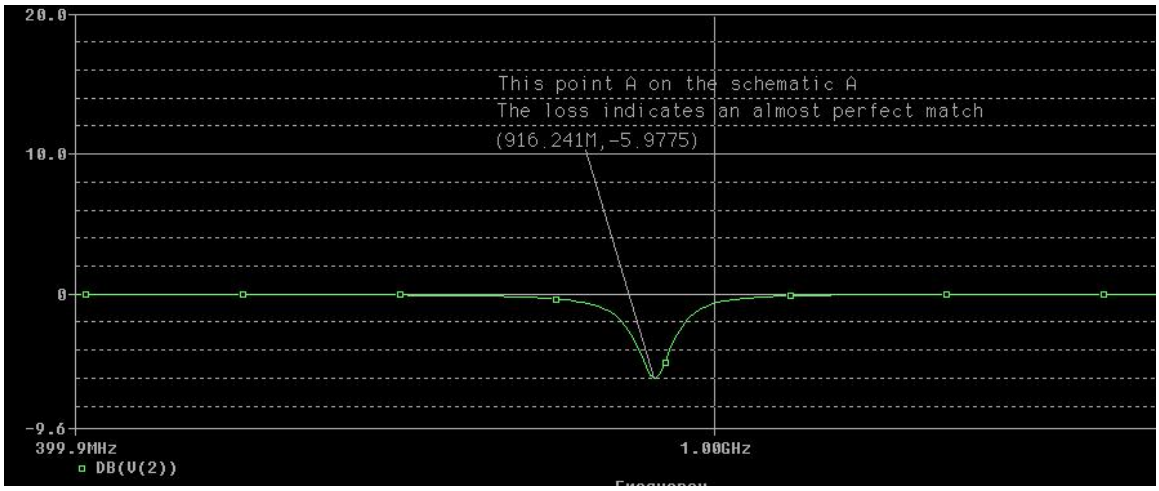
Xseries = -j18.3

This converts the schematic above to,



Note that the –j18.3 reactance cancels the j18.3 reactance leaving 7.98 Ohms matched to 8.0 Ohms at the input. *Therefore the signal at point A will be attenutated by 6 dB if the match is almost perfect.*

A simulation of the circuit is given below, which shows the attenuation at point A on the schematic A. For a match this point should be attenuated by 6 dB at the frequency of interest, 915 Mhz.



Simulation results from PSPICE

PSPICE .cir file for the simulation

The PSPICE cir file is given below.

R1 in 2 8
l1 2 3 31.9n

cm1 3 out 1.05pf
cm2 out 0 7.98e-12

rload out 0 50

****

*input signal

vin in 0 ac 1

****
.ac oct 100 100 50g
.probe
.end

Note: This technical memorandum was generated by the TechTeam at Signal Processing Group Inc. Signal Processing Group Inc., designs and manufactures highly cost effective analog and RF/wireless ASICs and modules using state of the art semiconductor, PCB and packaging technology. Please contact us at spg@signalpro.biz directly or through our website located at http://www.signalpro.biz.

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