General description: The SP42400P is a monolithic device fabricated in CMOS technology. Its generic function is to detect low to medium frequency, low voltage signals and provide an indication that such a signal has been detected. The device is divided into an analog front end consisting of two uncommitted operational amplifiers, a resistor divider, referenced to the power supply, which generates four equally spaced reference voltages, and a comparator which is referenced to these voltages through appropriate logic. The other functional blocks, which make up the SP42400P are a control logic block and two oscillators which are used to set the timing of the various functions of the device.

The SP42400P has two modes of operation. Mode one is activated when the FUN pin is at a logic '0'.This mode of operation is particularly suited to battery operation. A 16kHz high accuracy oscillator controls the timing of the output. This oscillator is made up of a comparator switching between two reference voltages derived from the supply (VDD). The MC pin is the positive input to this comparator. An external RC charging circuit, connected to this pin determines the oscillator frequency. With a 16Khz frequency, the output of the event detector will stay high for 30 seconds after an event is sensed. This conserves battery power. In this mode the pin SCHIN, is tied to VDD.

Mode two is intended to be used when the event detector is powered from a line derived supply. Mode two is selected by applying a logic '1' to the FUN pin. This allows the timing of the output to be determined by the frequency of a Schmitt trigger oscillator. This is advantageous if one wants the output to stay high for a time longer than 30 seconds. This timing can be programmed for this mode of operation. In this mode of operation, the 16 kHz clock still runs, but does not control the timing of the output. A delay time of 5 seconds or less to over 30 minutes can be programmed by the use of external RC components. (The R can be made variable if continuously programmable timing is desired).

In mode two operation, the INH pin can have an effect on the operation of the device. If a logic '1' is applied to INH, the circuit is disabled.

Analog Input Characteristics: The Event Detector is designed to be used in conjunction with an external sensor to provide an analog input signal. Optionally another sensor or control input can be used which supplies a logic level signal to the INH input.

The input analog signal is typically small (< 1mV). It is expected that some noise will be present on this signal. The uncommitted amplifiers on the device are used with external components to build an appropriate filter to filter this noise. The amplifiers are referenced to half the supply (HVDD). The first amplifier input is OP1IN and output OP1OUT. The second amplifier input is OP2IN, with a corresponding output OP2OUT.

The signal from OP2OUT is compared to reference voltages derived from the supply (VDD). There are four reference voltages, equally spaced from the supply to ground. For an event to be declared, the output OP2OUT must exceed a peak to peak value set by the topmost and lowest reference. The signal then enters a comparator, which compares these voltages. The output of the comparator then sets off events which lead to an output being generated and all the timing being initiated.

Pin Names and Functions

Pin	Name	Description
1	OUT	This is the logic level output of the SP42400P. When an event is detected this pin is forced to a logic '1'. For a 10 Volt power supply, this pin is capable of sourcing/sinking up to 20 mA at Vol and Voh.
2	VDD	This is the power supply pin. Typical values are in the 4 to 10 Volt range, while the supply current IDD is typically 100 uA.
3	OP2OUT	This is the output of the second uncommitted operational amplifier.
5	OP1OUT	This is the output of the first uncommitted amplifier. These amplifiers are typically used to pre-condition the analog input to the rest of the circuitry in the Event Detector. Filtering, gain or other adjustments are possible by using these amplifiers. High values of feedback resistance is highly recommended.
4	OP2IN	Input of the second op amp.
6	OP1IN	Input of the first op amp. Both these pins are connected to the inverting inputs of the op amps. The non - inverting inputs are connected to half the supply voltage. A bypass capacitor from HVDD is highly recommended as a noise bypass.
7	HVDD	HVDD is a voltage derived from VDD through a resistor divider internal to the device. A large capacitor should be connected to this pin to filter VDD noise, thus keeping power supply glitches from saturating the amplifiers.
8	MC	This is the inverting input, referenced to a fraction of VDD, to the Master Clock Comparator. An external resistor from VDD to this pin, and an external capacitor from this pin to VSS form a precision relaxation oscillator. These external components should allow this oscillator to run at 16 kHz.
9	VSS	This is the common or ground pin
10	MR	This is the master reset pin. During mode 1, when MR goes high, the circuit follows an initializing sequence: output at '1' for 2 seconds, then at '0' for 30 seconds, back to '1' for 1 second, and finally at '0'. This can be helpful for resetting or initializing other devices which may also operate within the users system. For mode two operation, the output is kept low for 32 seconds, regardless of activity detected by the input sensor, and thereafter the circuit is ready to be activated.
11	SCHOUT	This is the output of a CMOS Schmitt trigger inverter. This inverter is configured as a relaxation oscillator by connecting a resistance from SCHIN to SCHOUT, and a capacitance from SCHIN to VSS. During mode one, the oscillator is idle and during mode two it should be running at an adjustable frequency from 1 to 400 Hz. An external potentiometer from this pin to SCHIN can control the frequency.
12	SCHIN	This is the input to the Schmitt Trigger Inverter.
13	INH	A logic '1' on this pin inhibits circuit operation. It does not affect mode 1 operation.
14	FUN	A logic '0' on this pin sets mode one and a logic '1' sets mode 2.

Absolute Maximum Ratings

Symbol	Description	Value	Units
VDD	Power Supply Voltage	-0.5 to 12.0	Volt
VIN	Voltage at any input	-0.5 to VDD +0.5	Volt
VOUT	Voltage at any output	-0.5 to VDD + 0.5	Volt
IL	Latch up current	100	mA
T	Operating Temperature	90	Centigrade

Electrical Characteristics

SYM	Description	Conditions	Min	Typ	Max	Units
HVDD	Half VDD			50%		VDD
Vol	Digital Low LogicOutput				10%	VDD
Voh	Digital High LogicOutput		90%			VDD
Vih	Digital High Logic Input		90%			VDD
Vil	Digital Low Logic Input				10%	VDD
V1	Input Voltage to Op Amp 1			1.0		mV
Ii	Input Current	T=0 deg C T=70 deg C	-2.5 -10		2.5 10	uA uA
Ioh	Output High Current at pin 1	VDD > 7 Volt T = 70 deg C	20			mA
Iol	Output Low Current at pin 1	VDD > 7 Volt T = 70 deg C			-20	mA
fsch	Schmitt Trigger Frequency	Device operating in Mode two	1		400	Hz
fmo	Master Oscillator Frequency	When in mode 1, the master clock controls the circuit	13.3	16	20	kHz
Hsch	Schmitt Trigger hysterisis	Assuming perfect power supply	6.25		1.25	Volt

Notes:

Analog Specifications

SYM	Description	Conditions	Min	Typ	Max	Units
Vos	Input offset voltage	VDD = 10 Volt T=25 deg C.	-20			mV
AVOL	Open loop gain	VDD = 10 Volt T = 25 deg C	50			dB
Tprop	Propagation Delay	For 10 mV overdrive			100	us
Tcomp	Comparison Time				100	us
Tacq	Acquisition Time				100	us
VHYS	Hysterisis	These limits are derived through a resistor bridge. the hysterisis depends linearly on the supply. VDD = 10 V	-4.75		5.25	Volt
Vrefn	Reference Voltage thresholds	These limits depend linearly on the power supply. VDD = 10 V	3.3 4.3 5.3 6.3		3.7 4.7 5.7 6.7	Volt Volt Volt Volt

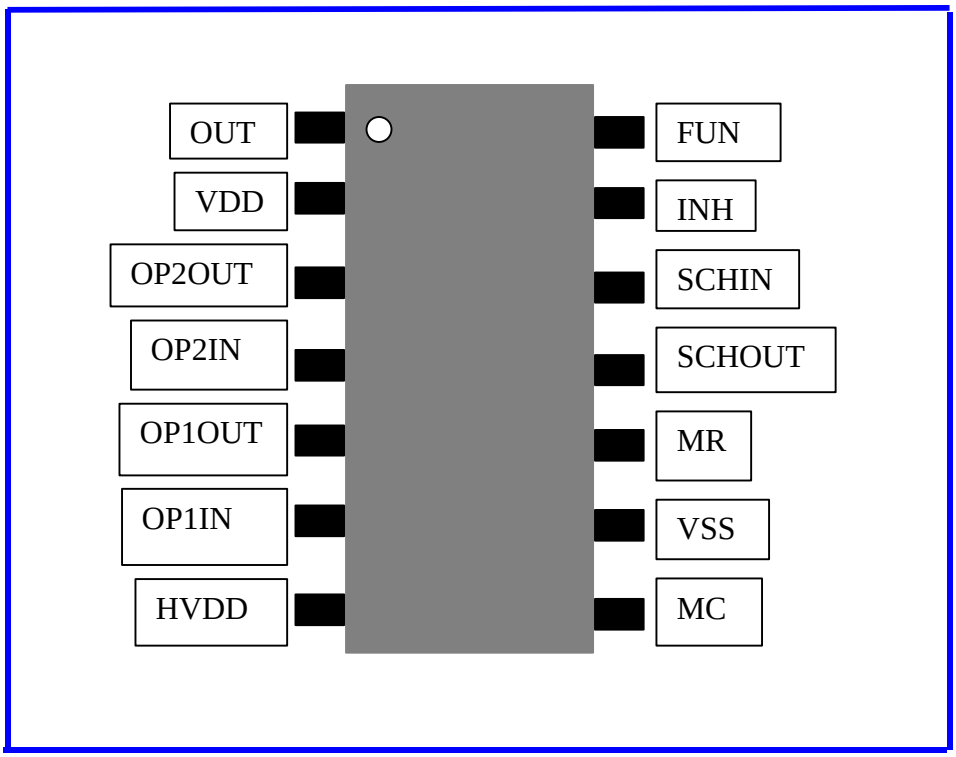
Operational Amplifier Essential Specifications

SYM	Description	Conditions	Min	Typ	Max	Units
Vos	Input Offset Voltage		-20		20	mV
AVOL	Open loop gain	VDD = 10V T = 25 deg C	50			dB
GBW	Gain bandwidth		0.1			MHz
SR	Slew rate		40			mV/us

Notes:

Packaging:

The SP42400P is packaged in a 14 pin DIP (or custom packaging in SOIC or bare die available)
The package diagram is shown below

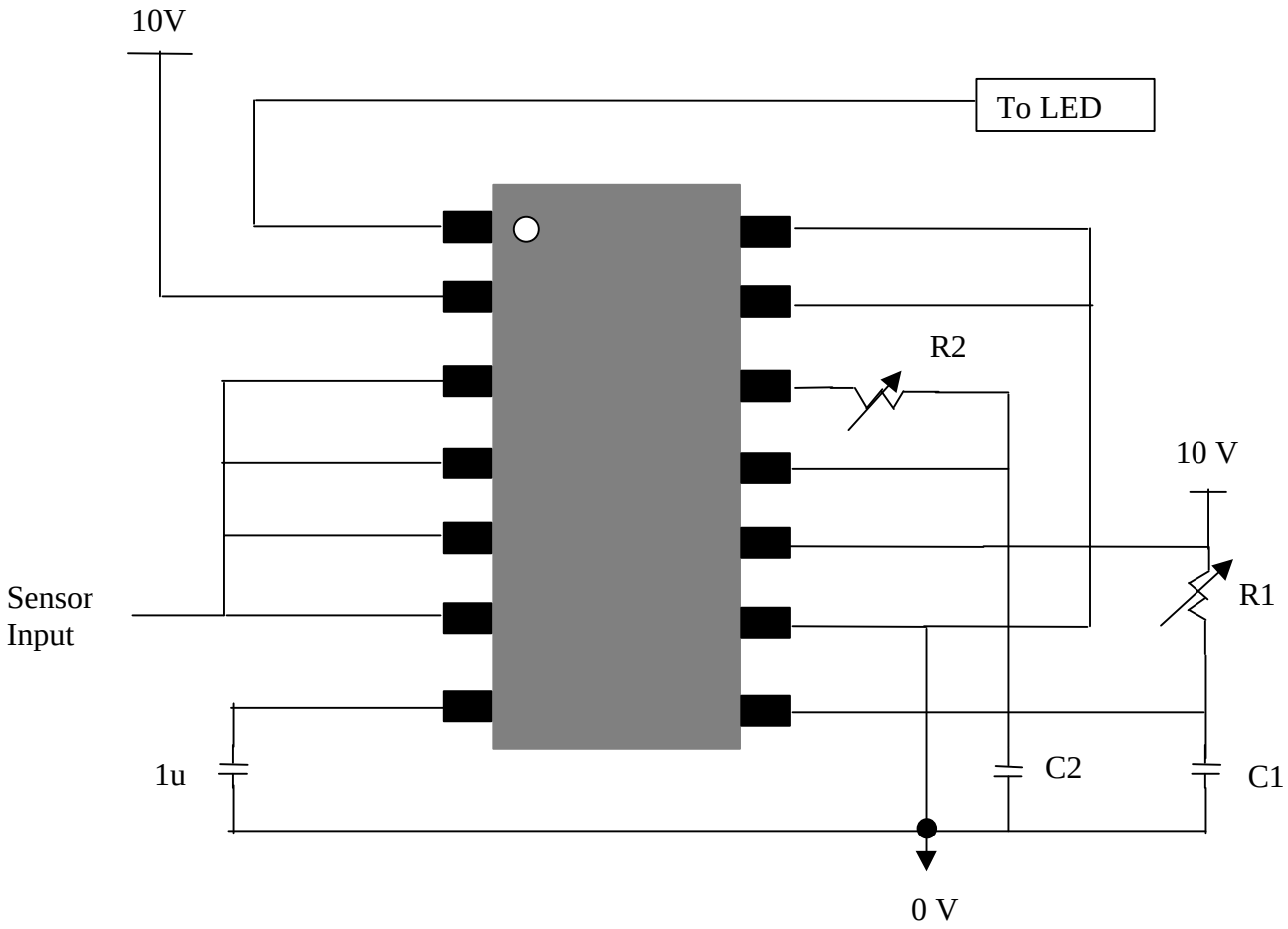


Applications: The Event Detector is a device that detects events or detects low voltage signals generated by a variety of sensors. Its INH input can be used to inhibit operation when not needed. In addition the timing of the output is controlled by the RC time constants which are generated by external components. There are two modes of operation that can be programmed simply by applying a logic input to the FUN pin. Because of this there are a number of generic applications which can addressed by the SP42400P. Some of these are sketched in the following pages with brief descriptions. Ultimately, of course the application is up to the user's ingenuity and engineering judgement. The descriptions below may trigger ideas about usage and are presented with that in mind.

Note:
Many of the active circuits that are used as peripherals can be implemented with the Event Detector as a core in a custom IC if the user feels that it is worthwhile. The Event Detector belongs to a category, within SPG's line of macrocells,(i.e. ready to use ICs, which can be

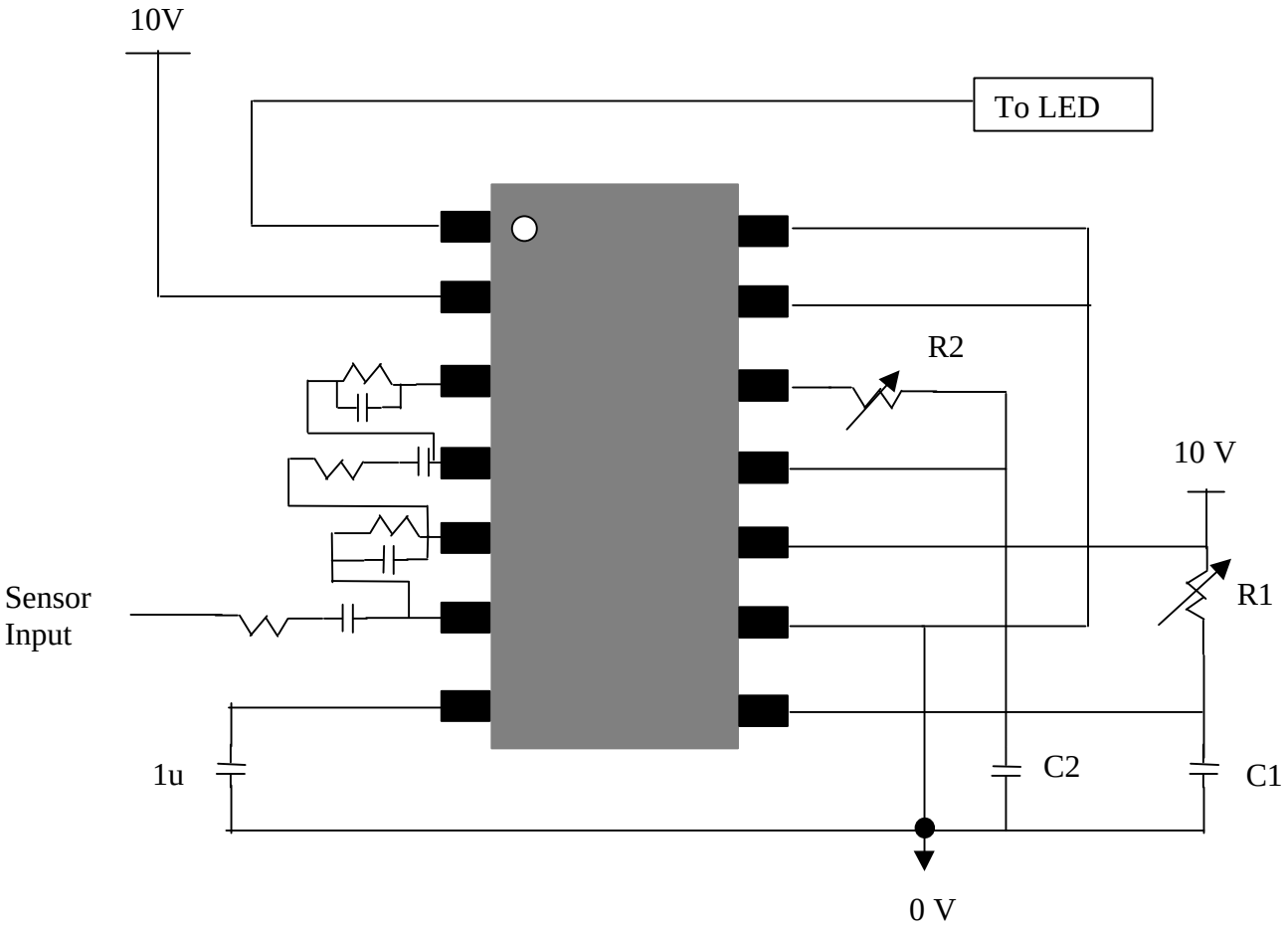
integrated with additional peripheral circuitry), to form larger and more complex devices at relatively low risk. Please call SPG or inquire about this and about low cost prototyping using the SP42400P as a core with other active circuitry as a custom chip for unique applications in your system.

Application 1: Simple Event Detector. In this case there is no preconditioning of the input. The uncommitted amplifiers are connected as unity gain followers. The output signal drives a LED to indicate an event. The input signal must traverse the entire range of the internally generated reference voltages before an event will be detected. R1 should be an adjustable resistance so that the frequency of the oscillator can be set to 16 kHz. R2 and C2 should be chosen such that the Schmitt trigger oscillator frequency is between 1 and 400 Hz depending on the delay required. This configuration can be used to detect relatively large signals.



Notes: The output driver at the OUT pin can drive a relatively large current of approximately 20 mA. So it can be used to drive latching relays, small motors, lamps or other load as long as the load current is within 20 mA. If a larger drive current is needed consider integrating a high power buffer with this event detector macrocell and make a custom circuit out of it if volumes of product warrant it.

Application 2: Event Detector with pre - conditioning. In this case the event detector is configured with a bandpass filter at the input. All other parameters remain the same. The bandpass filter rejects out of band noise.



Many other unique applications are possible using these basic configurations as building blocks. for example:

Application 3: Connect a four channel mux to the input of the sensor and four flip flops to the output. Using some extra logic drive the mux so that it samples one sensor after another. The clocking is configured to clock the results of the sensing into the individual FFs.

The types of applications are really a function of the user's imagination. In case of more complicated configurations the extra circuitry can be attached to the core event detector cell and integrated as a custom circuit if required to reduce board space or to lower cost.