A 0 to 3.3V to 0 to 15V level shifter for mixed voltage CMOS circuits

Principle of operation:

The input signal is applied simultaneously to the low voltage inverter and the left side high voltage n-channel MOSFET. If the input signal is at 3.3V the LV inverter output is ~0V. This causes the right hand side HV n-channel to turn OFF. The left hand side HV n-channel turns ON. This action causes the gate of the right hand side HV p-channel to go low thereby switching it ON. The gate of the left hand side p-channel then goes high causing it to switch OFF thereby causing OUTB to go low. The complementary output OUT goes high. The opposite is true when the input goes low. This is true CMOS level shifting and the only DC power dissipated is during switching.

Notes: Got to make sure that the HV p-channels are large enough to overcome the low impedance of the n-channels in the steady state before a new state can be established. Otherwise the change of state is not guaranteed.