Settling Times of two stage CMOS operational amplifiers Explanations and MATLAB M - FILES.

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Introduction: The most commonly used configuration for CMOS operational amplifiers is the two stage amplifier. There is a differential front end which converts a differential voltage into a current and a common source output stage that converts the signal current into an output voltage. An important criterion of performance for these op amps in many applications is the settling time of the amplifier. This may be defined as the time it takes for the output to settle to within a given error band after a sudden application of a step at its inputs. Typically a number 0f 0.1% is used. Even tighter tolerances may be used for critical applications.

This paper addresses a means to calculate settling time based on fairly simple equations developed to do so (IEEE Journal of Solid State Circuits, Vol SC-17, No. 1, February 1982, pp 74 to 80, by C.T Chuang). The complete set of equations is not used. Instead only the equations for overdamped response are used. These equations were further used to write a set of MATLAB M - FILES that are included with this paper.

Explanations: There are two basic parts in the settling time of CMOS amplifiers. The Slewing period and the linear period. During the slewing period, the input differential stage is so overdriven that it begins limiting action. During this time the Slew Rate (SR) is given by:

$$SR = Io/Cc. \tag{1}$$

Here Cc is the compensation capacitor of the op amp and Io is the tail current of the differential pair. The time for slewing is given by:

$$Ts \text{ Approximately} = (V - Io/gm1)/SR \tag{2}$$

where gm1 is the transconductance of the differential input pair and V is input differential step.

After this initial slewing period Ts, the amplifier operates in its feedback configuration with the loop closed. During this time it operates in the linear region. For the overdamped case the complete settling time is described by the following:

$$T1 = Ts + 1/(wn(d - sqrt(d^2 - 1))) \tag{3}$$

$$T2 = (d + sqrt(d^2 - 1)) \ 1000 \ Io \tag{4}$$

** The factor 1000 is for 0.01% settling accuracy.

$$T3 = (2.0*sqrt(d^2 - 1)) \ gm1V \tag{5}$$

$$Tset = Ts + T1[ln (T2/T3)] \tag{6}$$

the explanations of the factors d and wn are as follows:

d: d is the damping factor.   If d = 1, the system is critically damped.
                                       If d > 1, the system is over damped.
                                       If d < 1, the system is oscillatory.

(For further detailed treatment of feedback systems, see "Automatic Control Systems "
by Benjamin C. Kuo, Prentice - Hall Inc.)

We usually choose d = 1.1 to 1.2 for over damped response which may or may not be a good
number for your applications. The closer you get to d<1, the longer it takes to settle and the more
oscillatory the response becomes.

wn: wn is the natural undamped frequency. If d is = 0, the step response of the closed loop
amplifier is purely oscillatory. and the response will be sinusoidal. The factor wn corresponds to
the frequency of this undamped sinusoid. i.e. you should see a sinusoid at the output of an op
amp if you choose d = 0, or, which is more likely an error caused d in the amplifier to become =
0. The frequency at which the amplifier oscillates will be wn.

In the case of the CMOS op amp, the factors d and wn are related to the design parameters of the
amplifier as follows:

The fundamental design parameters of the two stage CMOS op amp are :

gm1 = the transconductance of the differential input stage = 2.0 *[sqrt(2.0*B*Ids)] where, B is
the product of the Intrinsic Transconductance of the input transistor and the Aspect Ratio (W/L).
Ids is the dc bias current through the transistor.

R1 = the output impedance of the input differential pair

C1 = the output load capacitance seen at the output terminals of the input differential stage.

Cc = the compensation capacitor used for gain/phase margin.

gm2 = the transconductance of the second stage of the amplifier, calculated as shown above for
the second stage gain device and bias current.

R2 = the output impedance of the second stage of the amplifier.

C2 = the capacitance seen at the output of the amplifier which also be partly (or usually is the
load capacitance)

Then,

wn^2 = (gm1/Cc)(gm2/C2) = (gm1*gm2)/(Cc*C2)   (7)

This expression is used to obtain wn.

d = [sqrt(gm2/C2)]/2.0*[sqrt(gm1/Cc)]   (8)

This equation is valid as long as the compensation capacitor Cc and the load capacitor C2 is
much larger than the small parasitic capacitance seen at the output of the input differential stage.
This is the case in practice.

An implication of eqn.(8) is that :

$$d > 1 \text{ if } Cc > 4.0*(gm1/gm2)*C2$$
$$d < 1 \text{ if } Cc < 4.0*(gm1/gm2)*C2$$
$$d = 1 \text{ if } Cc = 4.0*(gm1/gm2)*C2 \qquad\qquad (9)$$

In our case d > 1.

Having defined these parameters, we can now understand and use the MATLAB M - Files.